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E^2CL Nanosecond Logic System: Design Considerations for Elements and Interconnections

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Nanosecond logic necessitates both the design of a fast logic gate and the arrangement of versatile transmission line interconnections. In this article, the various methods of arranging transmission lines with different types of logic gate are considered. The advantages of the Mullard E^2CL system compared with the conventional CML system are described with particular reference to parasitic capacitance, temperature compensation and noise margin, input capacitance, output impedance and power consumption.

Ten Mullard E^2CL integrated circuit devices are described in detail. These devices consist of seven circuits concerned with the gating and the transmission of logic signals along transmission line interconnections, a Set-Reset Staticisor, a J.K. flip-flop, and an interface circuit to enable E^2CL to be driven by other logic systems.

INTRODUCTION

Development, in fields such as multi-access computing, telecommunications and high-speed instrumentation have created a demand for fast logic systems which are capable of operating with clock rates up to 100MHz. To meet this demand much research has been performed to create a logic gate capable of operating at 100MHz, to establish the best methods of interconnection, and to provide an overall system which is capable of being speeded up even further as the relevant technology is improved. The outcome of this research has been the Mullard E^2CL range of logic gates and the provision of information to enable optimum interconnections to be arranged between E^2CL gates. The present article describes the special factors which affect circuit design for high-speed switching, and how the E^2CL system meets the stringent demands for fast gates and suitable interconnections.

Special Aspects of Nanosecond Logic

When logic gates are designed to provide propagation delays of two or three nanoseconds or less, the switching edges must be about two nanoseconds or less. Under these conditions, two main problems arise; these are, first, the design of a gate for this switching speed, and, second, the design of suitable interconnections between two logic gates. The latter problem of interconnections arises because the natural propagation time for the pulse along about 40cm of interconnection is of the same order of magnitude as the voltage rise-times being considered.

One important implication is that the connections between gates cannot be left to chance, even when suitable gates have been provided. The connections must be treated as transmission lines, and cannot be treated as short-circuit connections with capacitance to ground, as they could be for lower edge speeds. One of two consequences may arise if the interconnections are not treated and terminated properly as transmission lines. One is that the pulse applied to the line connection may be so degraded at the input to the next gate that the gate fails to respond in time. Alternatively, reflections occur at the input to the second gate and return to the input of the line; the line connection, in effect, 'rings'; this may then cause spurious response of any other line connection to the same point, and cause spurious operation of other gates.

The gate input and output impedances must be chosen in such a way that the transmission line is suitably terminated in one of the several ways which are possible. In addition, since fan-out and fan-in are essential to any computer system, the effect of loading the transmission lines with gates must be carefully examined and allowed for in the gate design.

The practical construction of a computer may require the use of various forms of transmission lines, including coaxial cable, twisted or parallel pairs, printed circuit board transmission lines and multilayer board lines. The limits of the range of characteristic impedance of such lines must be taken into account in the design of a logic gate: in practice, values of characteristic impedance will be in the range 50Ω to 100Ω.

In a subsequent section of this article, the several possible methods of connecting to transmission lines are considered: these are examined in general terms, but in such a way that the factors which affect the choice of logic circuit may be more readily appreciated.

In choosing a general form of circuit upon which the basic gate circuit is to be constructed, it is necessary to make a choice between saturating and non-saturating logic circuits. In many ways the saturating logic offers advantages; in particular, the output and input voltage levels are more closely defined. On the other hand, at the high switching speeds being considered, hole-storage in the saturating transistors presents severe problems. For the latter reason, a form of current-steered non-saturating logic circuit has been chosen.

Other matters which need to be considered arise from the use of monolithic silicon integrated circuits. Since all of the circuit is within a small area of the silicon chip, the power dissipation has to be kept to an absolute minimum. The latter aspect is particularly important when the more complex items in the range of circuits are considered, because these require the interconnection of six to ten gates on a single chip. A satisfactory compromise must therefore be made between dissipation and the gate noise margin which unfortunately are opposing requirements. A closely allied problem is that of the parasitic isolation capacitance which is inherent in the present monolithic technology: the circuit must be designed to minimise the effects of these capacitances on the speed performance.

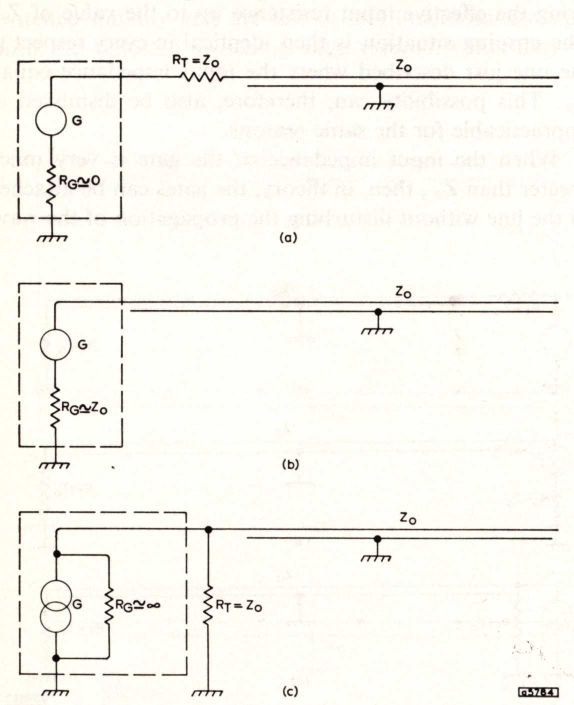

Fig. 1—Various methods of driving a single transmission line terminated at the sending end

Advantages offered by the integrated circuit include the fact the close tolerance between component values is inherent within the single silicon chip.

ARRANGEMENT OF TRANSMISSION LINES

The input and output impedances of the gate must be taken into account when transmission lines are used to connect gates. The many factors affecting the choice of high or low impedance in each case become clear if we consider the various ways in which a transmission line interconnection can in theory be arranged.

The choice of method of driving the line and providing suitable termination is complicated and is best considered in four separate contexts. First, consider the context of driving a single transmission line terminated at the sending end. Here, a low output impedance driver in series with the termination is equivalent in every way (Fig. 1) to a driver of output impedance equal to Z_0 with no terminating resistor. This can also be seen, by Norton's theorem, to be identical to a driver of high impedance in parallel with the terminating resistor. In any of the arrangements shown in Fig. 1, only a half pulse initially travels along the line, and it is a prerequisite of these systems that the far end must be effectively an open circuit so that the half pulse is reflected and doubled to provide full voltage on the line. The reflected half pulse returns to the sending end and is absorbed in the termination.

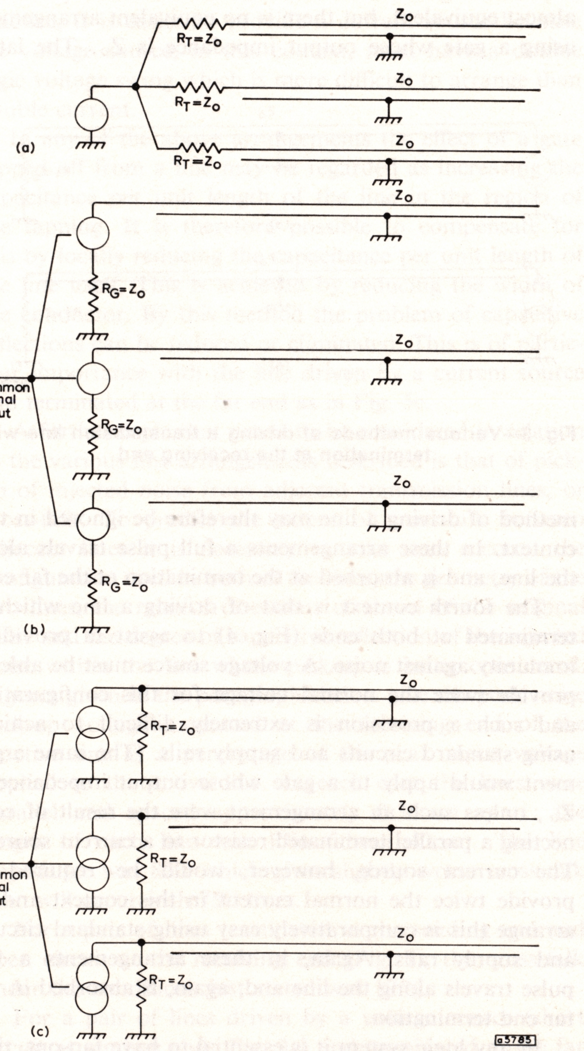

Fig. 2—Various methods of driving several transmission lines connected in parallel and with sending end termination

Secondly, in the context of simultaneously driving several lines in parallel, some differences appear (Fig. 2). The low impedance voltage source is in theory more flexible since it may drive several lines directly, whereas either of the other two systems demands additional isolated but identical output circuits. In practice, however, the power considerations of the voltage source limit the number of driven lines to two, and with only two lines the additional complexity of duplicating output circuits in the other systems is not severe. The advantage of the voltage source is therefore not great. Again, only a half pulse initially travels along these lines and the load must effectively be an open circuit so that the half pulse is doubled on reflection.

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Thirdly, there is the possibility of terminating the line at the far end. In this context (Fig. 3) the low impedance voltage source and the high impedance current source are almost equivalent, but there is no equivalent arrangement using a gate whose output impedance is Z_0. The latter method of driving a line may therefore be ignored in this context. In these arrangements a full pulse travels along the line, and is absorbed at the termination at the far end.

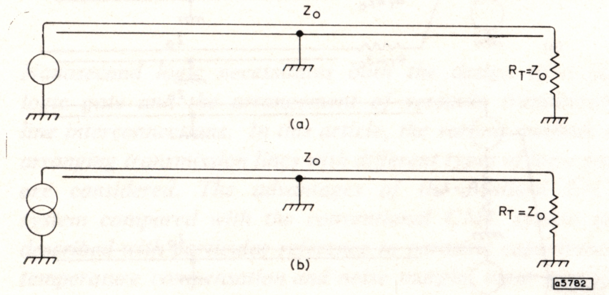

Fig. 3—Various methods of driving a transmission line with termination at the receiving end

The fourth context is that of driving a line which is terminated at both ends (Fig. 4) to assist in providing immunity against noise. A voltage source must be able to provide twice the normal voltage for this configuration and such a provision is extremely difficult to achieve using standard circuits and supply rails. (The same argument would apply to a gate whose output impedance is Z_0, unless such an arrangement were the result of connecting a parallel terminated resistor to a current source.) The current source, however, would be required to provide twice the normal current in this context and to arrange this is comparatively easy using standard circuits and supply rails. Again, in these arrangements a full pulse travels along the line and, again, is absorbed in the far end termination.

In any logic system it is essential to have fan-out, that is, each output must be capable of driving more than one gate. Therefore, before attempting to conclude which of the four above mentioned methods of arranging lines is the most viable solution, it is necessary to examine the various methods by which a number of gates can be connected to the output of one gate.

It is convenient to consider the loading of the output of a gate under the three conditions that the input of the driven gate could present: the input impedance of the gate may be equal to, less than, or greater than Z_0, the characteristic impedance of the line.

When the gate input impedance is equal to Z_0, only one gate can be placed at the end of each line or mismatching will occur. Consequently, a fan-out can be achieved only by driving several lines simultaneously, each line terminated in a single load. This corresponds to the receiving end termination of Fig. 3 used in the fan-out method of Fig. 2, and can provide only a very limited fan-out. In practice, power dissipation would limit the fan-out to two or three. The possibility of gate input impedance being equal to Z_0 can therefore be dismissed as being impracticable.

When the gate input impedance is less than Z_0 it would be necessary to add series resistance at the input to bring the effective input resistance up to the value of Z_0. The ensuing situation is then identical in every respect to the one just described where the input impedance equals Z_0. This possibility can, therefore, also be dismissed as impracticable for the same reasons.

When the input impedance of the gate is very much greater than Z_0, then, in theory, the gates can be attached to the line without disturbing the propagation of the wave along the line. Even allowing for the finite impedance in this case it is still possible to use a practical gate impedance greater than Z_0 with any of the line arrangements described above, or any of the variants produced by combining parts of them.

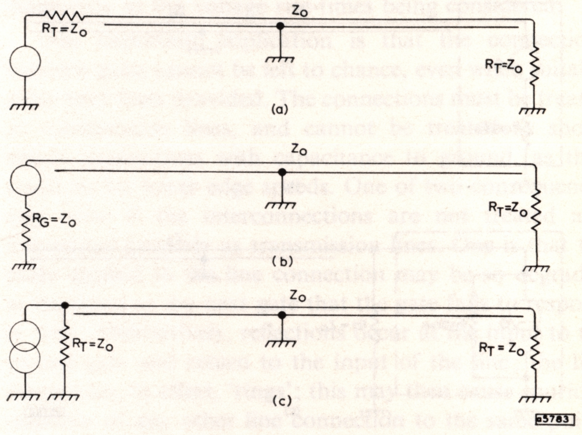

Fig. 4—Various methods of driving a transmission line terminated at both ends

The only usable value for gate input impedance is therefore one in excess of Z_0. The finite impedance will, in practice, cause some disturbance of the propagated wave. Whatever d.c. resistance the gate input has, there is inevitably some parallel input capacitance and this capacitance is the cause of the disturbance of waves propagated along the line. The switching edge must charge this capacitance and the capacitance therefore appears temporarily as a near short circuit: the charging process affects the progress of the wave. The effect is that the switching edge deteriorates and assumes a slower rise or fall time. A secondary effect is that, from intermediate gates along the line a spike pulse in the opposite sense to the switching edge is reflected back along the line to the sending end: if this capacitive reflection is of sufficiently large amplitude and duration, temporary reversal of switching of other gates along the line may occur.

When practical gates of input impedance greater than Z_0 are fanned out from a driving gate, then certain restrictions have necessarily to be applied to the line arrangements discussed earlier to allow for the deterioration of switching edge and capacitive reflections. In the layout of Fig. 1, the load must be restricted more or less to the far end of the line if simultaneous switching of the driven gates is required, because only a half pulse initially travels along the line. The capacitive reflection is absorbed in the termination at the sending end. If a distributed fan-out is applied to this line then the first gates are only half-switched initially and are left in this indeterminate state until the reflected switching edge returns. (This may be acceptable in some applications.) Similar restrictions are imposed on the fan-outs with the layouts shown in Fig. 2, for the same reasons.

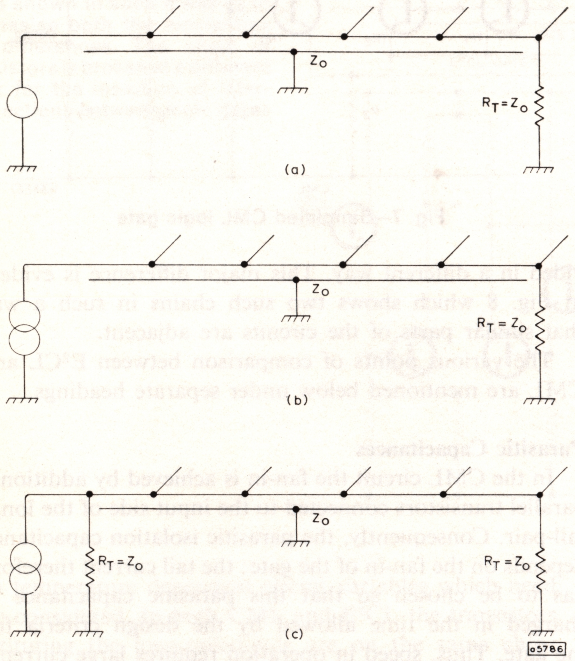

Fig. 5—Distributed loading of transmission lines

When capacitive reflections are considered for a line terminated at the far end, differences appear between the line driven by a voltage source (Fig. 5a) and by a current source (Fig. 5b). In both cases a full pulse travels along the line, and so receiving gates can be tapped off all along the line. For the voltage source line (Fig. 5a) the capacitive reflections are reflected again at the sending end but they are in anti-phase at this second reflection and thus they travel along the line reinforcing the original switching edge. For the current source line (Fig. 5b), on the other hand, the second reflections are in phase with the backward travelling capacitive reflections and so travel along the line tending to reverse the original switching edge: this has been called 'the ping-pong effect'. Because of this tendency, the current source combined with a distributed load and far end termination can be allowed only a light total loading of receiving gates. For a receiving gate situated near the sending end, the reflections can become additive, increasing the likelihood of spurious switching. As a result, the voltage source in this configuration requires a time equal to twice the line delay to settle, compared with three times the line delay required by the current source.

If terminations are provided at both ends of the line, then all second reflection problems are avoided because all initial reflections are absorbed either at one end of the line or the other. This arrangement (Fig. 5c) may be driven by either a current source or a voltage source; in practice, it is easier to provide a current source because the voltage source, in this context, must have a double logic voltage swing which is more difficult to arrange than double current.

In any of the above arrangements the effect of a gate tapped off from a line may be regarded as increasing the capacitance per unit length of the line in the region of the tapping. It is therefore possible to compensate for this by locally reducing the capacitance per unit length of the line itself. This is achieved by reducing the width of the conductor. By this method the problem of capacitive reflections can be reduced or eliminated. This is of particular importance with the line driven by a current source and terminated at the far end as in Fig. 5c.

A further topic that needs to be considered in relation to the various line arrangements described is that of pick-up of injected noise from adjacent transmission lines, or cross-talk. To predict the extent of cross-talk between adjacent lines it is necessary to take into account the configuration used in both of the lines, the geometry of the two lines, the relative directions of travel of the original pulse and the degree of capacitive reflection of the injected noise within the line whose pick-up is being considered. Figures given in the paragraphs below give the peak noise pick-up voltage measured at the receiving end of the inactive line as a percentage of the peak input voltage applied to the active line. In each case the lines were parallel and spaced approximately 0·35mm apart: the length of each line was 17in (about 43cm). The line impedance was 82Ω which gives slightly worse cross-talk than will occur with 75Ω lines.

For a pair of lines terminated at the sending end and open circuit at the receiving end (Fig. 1), the cross-talk under the conditions just stated was 17%.

For a pair of lines driven by a voltage source (short circuit at sending end; Fig. 3a) and terminated at the far end, the cross-talk was 10% (in antiphase).

For a pair of lines driven by a current source (open circuit at sending end; Fig. 3b) and terminated at the far end, the cross-talk was 13%.

For a pair of lines terminated at both ends (Fig. 4) the cross-talk was 4·5%.

From these figures ability to terminate the line at both ends in a noisy environment is obviously desirable: this fact is an argument in favour of using current drive.

It has been intended to show in the above paragraphs that both the current source and the voltage source offer some advantages and both impose some limitations. It is therefore necessary to examine the designs of the available current-steered logic circuits to see which provides the optimum properties.

DERIVATION OF E²CL

A simplified form of the E²CL circuit for a single logic gate is given in Fig. 6. The relationship of this circuit to earlier current-steered logic will be discussed below. The circuit consists of a long-tail-pair TR_3 and Tr_4. One side of this pair is driven by the input signal via transistor TR_1 or TR_2: these are connected as parallel emitter followers and act as an AND gate for negative logic or an OR gate for positive logic. (The reader should consult page 159 for a definition of negative and positive logic.) The two voltage levels which may be applied as signals to the input are 0V and −0·7V. Thus, the base of TR_3 is set at −1·4V when both inputs (bases of TR_1 and TR_2) are at −0·7V, but the base of TR_3 is at −0·7V if either or both of the inputs are at 0V. The other side of the long-tail-pair is connected to a reference voltage derived in this simplified circuit from R_6 and R_7 by way of TR_5 acting as an emitter follower. The value of the reference voltage at the base of TR_5 is designed to be the mid-point of the logic voltage swing.

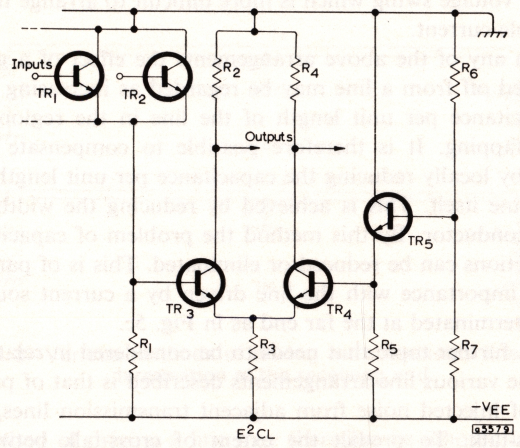

Fig. 6—Simplified E²CL logic gate

If, therefore, the input to either TR_1 or TR_2 is higher than the reference voltage between R_6 and R_7, the tail current flows through TR_3. Conversely, if the inputs of both TR_1 and TR_2 are below the reference voltage, the tail current flows through TR_4. The outputs are taken from the collectors of TR_3 and TR_4. The inverted output is available at TR_3 giving the NAND function for negative logic (and the NOR function for positive logic). The non-inverted output is available at TR_4, giving the AND function for negative logic (and the OR function for positive logic). The output is effectively a current output equal to the tail current.

E²CL has marked resemblances to the more conventional form of current-steered logic circuit (CML) shown in Fig. 7. In this simplified form of CML circuit the long-tail-pair consists of TR_3 on one side and TR_2 (or TR_1) on the other; the function of AND for negative logic or OR for positive logic is performed by TR_1 and TR_2. The emitter follower that constitutes the input in E²CL (TR_1 etc., Fig. 6) appears in the CML circuit as an output transistor (TR_5 in Fig. 7) which gives a voltage source output.

It will be appreciated that the major difference between E²CL and the conventional CML is the position at which the transistor chain is broken for the insertion of interconnections and fan-out arrangements: fan-in is also provided in a different way. This major difference is evident in Fig. 8 which shows two such chains in such a way that similar parts of the circuits are adjacent.

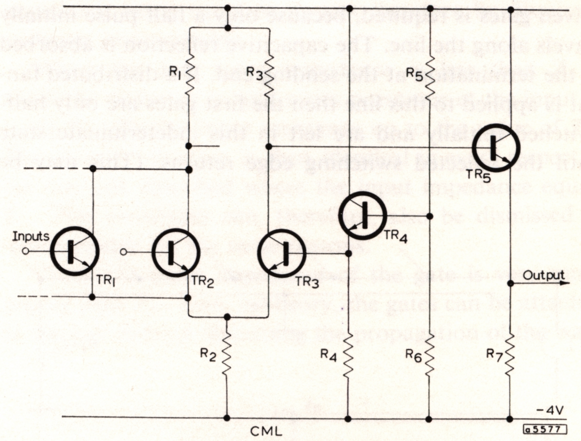

Fig. 7—Simplified CML logic gate

The various points of comparison between E²CL and CML are mentioned below under separate headings.

Parasitic Capacitances

In the CML circuit the fan-in is achieved by additional parallel transistors connected to the input side of the long-tail-pair. Consequently, the parasitic isolation capacitance depends on the fan-in of the gate: the tail current therefore has to be chosen so that this parasitic capacitance is charged in the time allowed by the design criteria for the gate. Thus, speed in operation requires large currents in this tail and the dissipation is accordingly high. Equally, the rise time and fall time for this gate will be dependent on fan-in unless the tail current is adjusted. A further problem is that since there is only one transistor on the reference, or bias driver, side of the pair, compared with two or more on the input side, the switching speeds will be different at the two output points, unless precautions are taken to balance capacitances: thus the AND/OR output will switch faster than the NAND/NOR output.

In the E²CL circuit there is a single isolation capacitance on each side of the long-tailed-pair. The tail current can therefore be designed to be at the minimum usable value, and the switching speeds at the outputs are automatically balanced.

The isolation capacitance of the fan-in in the E²CL circuit is effectively connected to ground and has little effect on the speed of switching.

Temperature Compensation and Noise Margin

The logic swing for both E²CL and conventional CML is approximately V_{BE}, and consequently the noise margin is approximately 250mV. The noise margin is a function of the temperature of the circuit, and also a function of the difference in temperature between successive interconnected gate circuits. The V_{BE} of the transistors are the main temperature dependent circuit variables which need to be considered. In both CML and E²CL the transistors constituting the long-tailed-pair are on the same chip: therefore the temperature difference between them is negligible, and changes in V_{BE} caused by changes in temperature are automatically balanced. Manufacturing tolerances in the V_{BE} of these two transistors can also be ignored for the same reason.

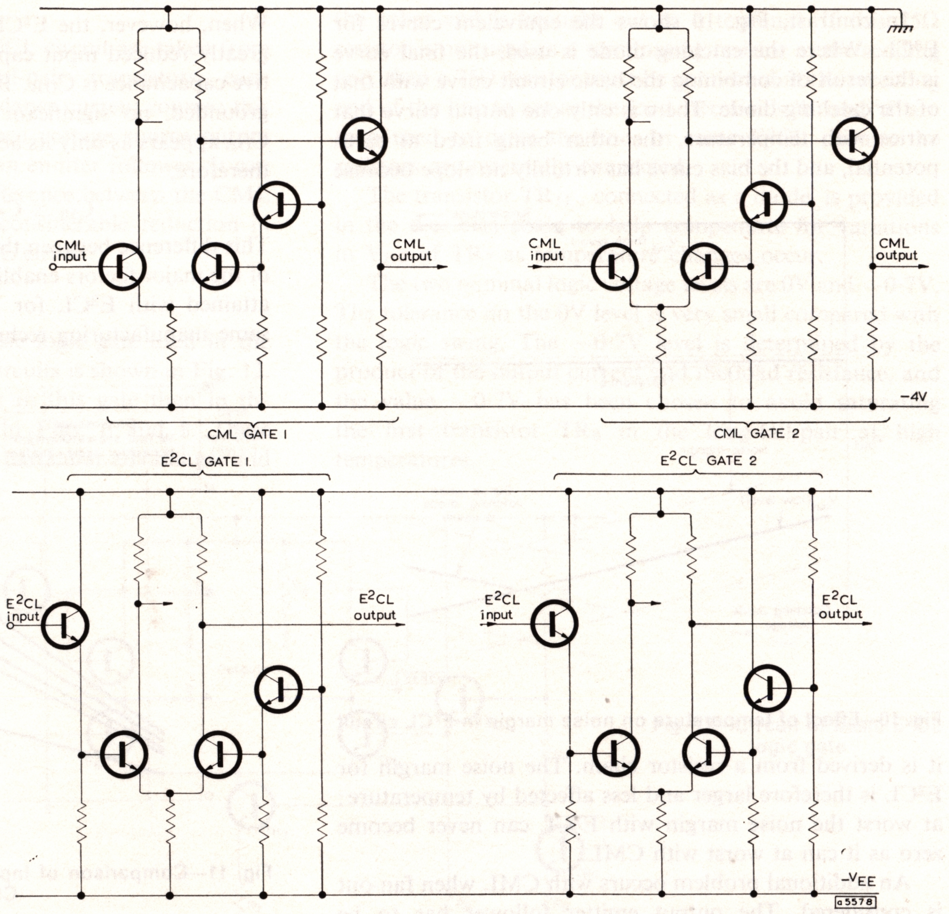

Fig. 8—Simplified E²CL and CML gates shown in such a way as to emphasise both the similarities and differences. The chain of transistors is broken at a different point for the insertion of interconnections between logic gates

In the E²CL circuit, the input emitter follower and the reference emitter follower are again on the same chip and have very similar loading. The manufacturing tolerances and the changes in V_{BE} caused by temperature variations are again automatically balanced.

In contrast, one of the relevant emitter followers in the CML circuit is on the output of the previous gate and therefore on a different chip. Therefore variation in V_{BE} caused by temperature differences and manufacturing tolerances in V_{BE} both subtract from the available noise margin in adverse conditions. This is true even when bias drive is provided within the gate circuits on the chip, rather than by a separate bias drive circuit.

The effect of temperature on the available noise margin in the CML circuit can be seen in Fig. 9. The three continuous lines represent the voltage of (top to bottom) the high level output, the reference bias drive, and the low level output. The discontinuous lines represent the tolerances on these three voltages because of device-to-device spreads: a measure of the noise margin is therefore shown by the gap between adjacent discontinuous lines. If the two connected gates are at substantially different temperatures the noise margin is further reduced and may become zero in severe cases: if the receiving gate is at temperature A, while the sending gate is at temperature B, the residual noise margin is indicated by the voltage range shown. The noise margin in the opposite state (high, in this example) is increased but it is the minimum value in either state that must be observed in practice.

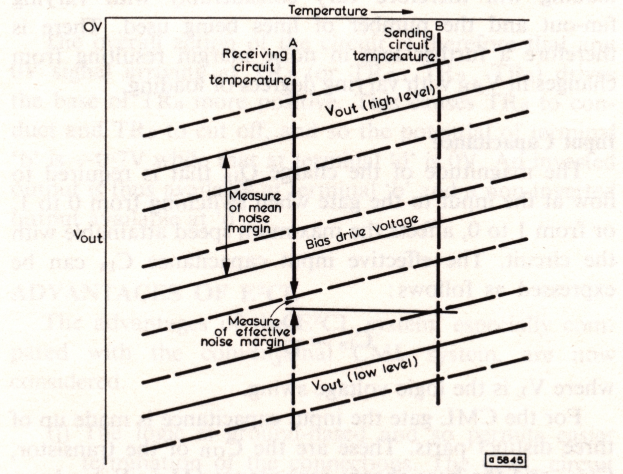

Fig. 9—Effect of temperature on noise margin in CML circuit

In contrast, Fig. 10 shows the equivalent curves for E^{2}CL. Where the catching diode is used, the final curve is the result of combining the basic circuit curve with that of the catching diode. There is only one output curve that varies with temperature, the other being fixed at earth potential, and the bias curve has virtually no slope because it is derived from a resistor chain. The noise margin for E^{2}CL is therefore larger and less affected by temperature: at worst the noise margin with E^{2}CL can never become zero as it can at worst with CML.

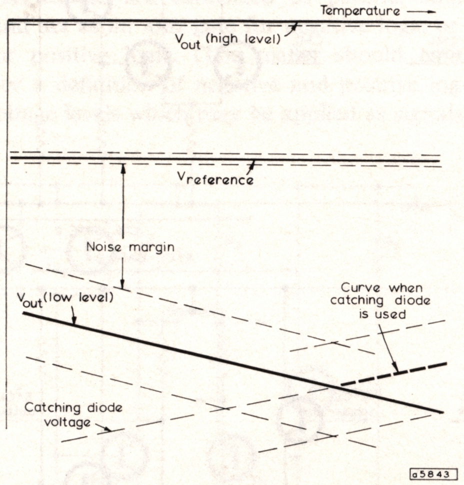

Fig. 10—Effect of temperature on noise margin in E^{2}CL circuit

An additional problem occurs with CML when fan-out is considered. The output emitter follower has to be designed to drive a terminated transmission line. The loading will therefore vary considerably with varying fan-out and the number of lines being used. There is therefore a further loss in noise margin resulting from changes in V_{BE} with varying degrees of loading.

Input Capacitance

The magnitude of the charge Q_{in} that is required to flow at the input to the gate when switching from 0 to 1, or from 1 to 0, affects the maximum speed attainable with the circuit. The effective input capacitance C_{in} can be expressed as follows:

$$C_{in} = \frac{Q_{in}}{V_L},$$

where V_L is the logic voltage swing.

For the CML gate the input capacitance is made up of three distinct parts. These are the C_{OB} of the transistor, C_{TE}, and the base charge capacitance $(\Delta I_c/\omega_t V_L)$, where, in this case, $\Delta I_c = I_c$. Since the collector voltage of the input transistor changes by an amount equal to, but in antiphase to, the logic swing, the capacitance C_{OB} is charged to twice the logic swing, and thus will appear, as a result of this Miller effect, as twice its actual value.

Similarly the emitter voltage swings through only half the logic swing and the value of C_{TE} will appear as only half of its actual value.

The total effective input capacitance for the logic swing in the CML circuit is therefore given by,

$$C_{in} \simeq 2C_{OB} + \tfrac{1}{2}C_{TE} + (\Delta I_c/\omega_t V_L) \simeq 8 \text{ to } 12\text{pF}$$

When, however, the E^{2}CL circuit is considered there is a greatly reduced input capacitance because the only effective capacitance is C_{OB}. Because the collector is effectively grounded, no significant Miller effect can occur and so C_{OB} appears as only its actual value. For the E^{2}CL circuit, therefore,

$$C_{in} \simeq C_{OB} \simeq 2 \text{ to } 3\text{pF}.$$

This difference between the CML and E^{2}CL circuits is one of the major factors enabling higher switching speeds to be attained with E^{2}CL for lower power dissipation, if the same manufacturing technology is used. Thus, for a given line impedance, three E^{2}CL gates can be driven for only the same degradation of rise time as is caused by driving one CML gate. Alternatively, for a given fan-out, the interconnecting line impedance for CML must be one third of that for E^{2}CL, with the consequent increase in dissipation in the circuit.

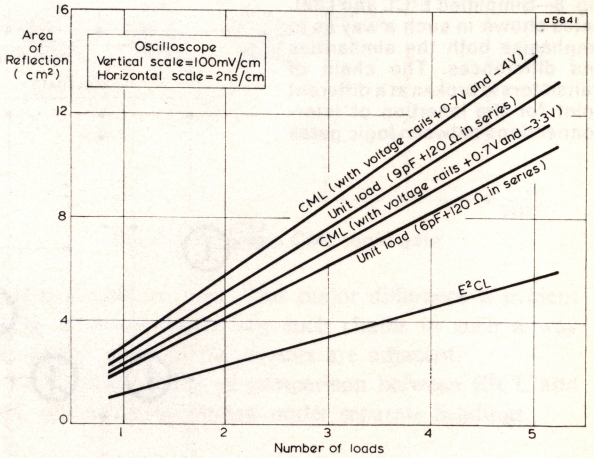

Fig. 11—Comparison of input capacitance of E^{2}CL gate and CML gate

The curves shown in Fig. 11 enable a comparison to be made between the loading effects of E^{2}CL and CML. The arrangement for making these measurements consisted of a gate driving approximately 2 ft (60cm) of transmission line which was terminated at the far end: loads were inserted at about the centre of the line and reflections were observed at the sending end. Two reflections occur, corresponding to the two switching edges. One of these reflections, however, is distorted by the action of the catching diode. The other reflection, which is undistorted, was used for measurements.

As the number of unit loads is increased at the loading point, the amplitude of the reflections does not increase proportionately. A closer examination of the waveform shows that the area of the reflection increases proportionately with the number of loads. This effect appears to be the result of a time constant in the circuit, consisting of the input capacitance and the series collector resistance.

The areas of the reflections were measured with various numbers of unit loads of E^{2}CL and CML circuits. The actual values of capacitance were computed by a substitution method, using known values of capacitance and making adjustments for the collector resistances.

Output Impedance

Because the outputs of the E^{2}CL circuit are taken from the collectors of the long-tail-pair transistors, each output is effectively a high impedance current source: this contrasts with the low impedance voltage source output in the CML circuit taken from an emitter follower. It can be shown that this particular difference between the CML and the E^{2}CL circuits gives a considerable reduction in power requirements for the E^{2}CL circuit.

THE E^{2}CL GATE

The actual circuit of the basic logic gate used in the E^{2}CL system of logic function circuits is shown in Fig. 12. Several more transistors appear in this gate than in the general circuits shown earlier in Figs. 6 and 8. These transistors are added to provide particular advantages and the reader should bear in mind that to construct a transistor in integrated circuits is often less difficult than to construct a resistor.

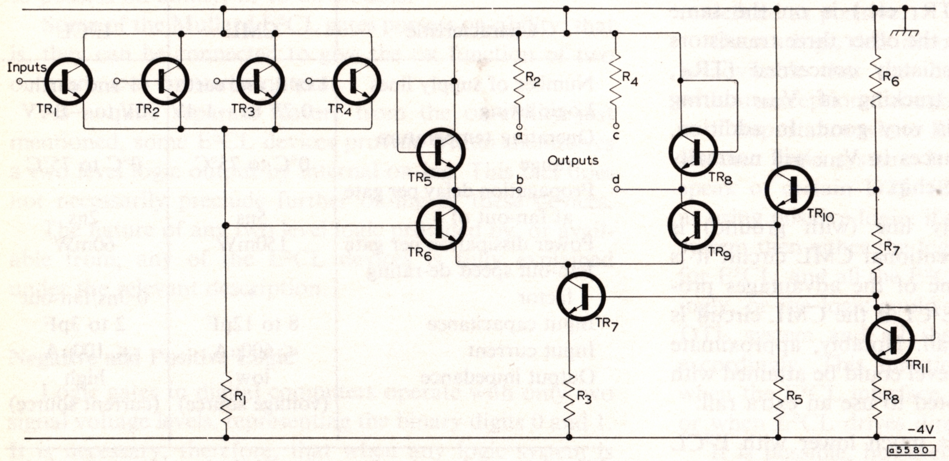

Fig. 12—Circuit of basic E^{2}CL logic gate

The input signal may be applied to any one or combination of TR$_1$, TR$_2$, TR$_3$ and TR$_4$. These act as emitter followers and the signal passes to TR$_6$ which constitutes the long-tailed-pair with TR$_9$. The load of TR$_6$ is a 75Ω resistor. The transistor connected as a diode for connection in parallel with the load, is an addition to the fundamental form of the circuit and acts as a catching diode. Similarly, the load of TR$_9$ is the 75Ω resistor, and the catching diode TR$_8$ is available. The purpose of the diode is to restrict the logic voltage swing to its correct value when several gates are OR-ed to one resistor (see OR-ing under FKH101, page 166), and is not used in those gates which cannot be OR-ed.

The current source transistor TR$_7$ in the tail of the differential pair TR$_6$ and TR$_9$ is primarily to ensure equality in the d.c. output currents in each state. This ensures that the same logic swing is produced across equal resistors. Additional advantages are that rise and fall times are balanced, and a low supply voltage can be used.

The outputs are taken with respect to ground from the output terminals 'b' and 'd', but, to obtain the correct logic swing there must be a 75Ω load. The resistors R$_2$ and R$_4$ have one end grounded and, in some E^{2}CL devices the other end is brought out to a terminal. If this 75Ω resistor is not used as a terminating resistor at the sending end, then a 75Ω resistor must be connected at the receiving end of the line to act as the load: terminals 'b' and 'd' are then used to drive the line. In some E^{2}CL circuits the resistors are internally connected.

The transistor TR$_{11}$, connected as a diode, is provided in the d.c. bias chain to help compensate for variations in V_{BE} of TR$_7$ as temperature changes occur.

The two nominal logic voltage levels are 0V and −0·7V. The tolerance on the 0V level is very small compared with the logic swing. The −0·7V level is determined by the product of the output current and the load resistance, and the value −0·7V has been chosen to avoid saturating the first transistor TR$_6$ in the long-tail-pair at high temperatures.

The overall action of the circuit is therefore that any 0V signal arriving at TR$_1$ (or TR$_2$, TR$_3$, TR$_4$) drives the base of TR$_6$ more positive. This causes TR$_6$ to conduct and TR$_9$ to cut off, and so the potential of terminal 'b' is −0·7V while that at terminal 'd' is 0V. An inverted output is thus available at terminal 'b' and a non-inverted output available at 'd'.

ADVANTAGES OF E^{2}CL

The advantages of the E^{2}CL system, especially compared with the conventional CML system, are now considered.

(i) The logic is ground-based and so permits easier termination of the connections. The CML circuit requires a third supply line (or what is effectively a third supply line obtained via a potential divider across the main supply lines) if virtual grounding of one logic level is to be achieved; extra power is dissipated in this way when parallel termination is utilised.

(ii) The input capacitance of the E^{2}CL circuit is smaller because the Miller effect is not significant in the input transistors; the collector is effectively grounded. This considerably speeds up the switching of the gate compared with CML.

(iii) The parasitic isolation capacitance of the transistors in the long-tailed-pair is caused by one transistor only on each side of the E^{2}CL circuit, and is balanced; it is not increased by fan-in. This gives balanced and faster switching times for a given power dissipation in the gate.

(iv) Because the input transistor conducts a lower emitter current, the base current is correspondingly reduced. In the case of a sending end termination, the d.c. fan-out of E^{2}CL will be larger than for CML. It is interesting to note that sending end termination requires minimum power in the possible configurations with CML.

(v) The output impedance of the gate is the same at both levels of output voltage, and so line termination can be accurately arranged.

(vi) The emitter follower (TR$_1$ etc.) is on the same integrated circuit chip as the other three transistors with which it is immediately concerned (TR$_6$, TR$_9$, TR$_{10}$), and so tracking of V$_{BE}$ during temperature variations is very good. In addition, the manufacturing tolerances in V$_{BE}$ will normally match each other on one chip.

(vii) Only one power supply line (with ground) is required. With the conventional CML circuit it is possible to produce some of the advantages provided automatically by E^{2}CL if the CML circuit is given an extra supply rail. Notably, approximate grounding of one logic level could be attained with conventional CML adapted to use an extra rail.

(viii) The power dissipation is much lower with E^{2}CL than with any comparable logic system. It is better than the apparently similar CML system primarily because the emitter follower is placed at the input of the circuit and consequently never has to drive a line and its fan-out. This emitter follower has an internal connection in E^{2}CL to the long-tail-pair and can have much reduced power because of this. The increased dissipation required in the long-tailed-pair to drive the line does not counterbalance this by any significant amount.

(ix) The E^{2}CL configuration inherently makes available both the inverted and the non-inverted output without extra power being required.

(x) Linking gates in parallel to provide the OR-facility is easily arranged with the E^{2}CL circuit. This is explained later in greater detail (see FKH101, page 166).

These advantages indicate that the E^{2}CL system provides a better power-speed product than CML. Interconnections can be properly arranged. Finally, it should be noticed that the system is inherently capable of being speeded up further as the manufacturing technology is improved.

COMPARISON OF E^{2}CL AND CML PERFORMANCE

It is worthwhile at this stage to compare the technical description of a conventional CML gate with that of an E^{2}CL gate. Strict comparison is not possible because the exact figures would depend on the details of the design and technology used, but the figures given in Table 1 indicate the relevant performance achieved, assuming the same manufacturing technique is used in each case, and show the advantage of E^{2}CL where high speed logic is required.

Some of the figures given in Table 1 are strongly interdependent. In particular, the method used in fan-out effects the fan-out figures and the propagation delay times. These are discussed, however, in more detail in the succeeding pages.

TABLE 1

Comparison of CML and E^{2}CL Gates

Characteristic	CML	E^{2}CL
Number of supply lines	1 or 2, and earth	1 and earth
Logic swing	−0·7V to −1·4V	0V to −0·7V
Operating temperature range	0°C to 75°C	0°C to 75°C
Propagation delay per gate at fan-out of 3	5ns	2ns
Power dissipation per gate	150mW	60mW
Fan-out speed de-rating factor	*	0·3ns/fan-out
Input capacitance	8 to 12pF	2 to 3pF
Input current	⩽ 600μA	⩽ 100μA
Output impedance	low (voltage source)	high (current source)

*The fan-out de-rating factor for CML depends on the design of the emitter follower and the type of interconnection employed, but will generally be significantly higher than the factor for E^{2}CL.

THE RANGE OF MULLARD E^{2}CL DEVICES

The initial range of ten E^{2}CL devices consists of six logic circuits, one line receiving circuit, two staticisors and an interface unit. These ten devices are described briefly on pages 159 and 160, and are described in more detail subsequently, but for the sake of clarity some of the concepts and terms used there are defined here.

Levels of Logic

Each of the four basic logic functions (AND, NAND, OR, NOR) is said to be an operation at one level of logic. In practice it is essential to use combinations of these functions, and operations which result from the use of any two of the basic functions are said to be operations at two levels of logic. It is evident that from these four single level functions, it is possible to form sixteen two level functions. Some of these sixteen functions are precisely equivalent to others, and in any case, some of the functions are more useful in practice than others.

In the E^{2}CL range the standard logic gate provides both AND and NAND outputs for negative logic (see page 159). To attain a useful two level logic function it is required to perform the OR operation on two or more AND or NAND outputs. This facility is available in some of the E^{2}CL gates by arranging suitable connections between gates. Two level logic operation is also performed by some of the E^{2}CL gates as a permanent feature resulting from various internal connections made during manufacture. These facilities are described in detail in the sections on the relevant devices.

OR-ability

To provide two level logic with a basic AND or NAND gate it is necessary to combine gates in some way so that the output from either one gate or another produces an output at a given point of interconnections. For the purposes of this article, the gates are then said to have been OR-ed. For the basic gate circuits to be capable of being interconnected in this way, they must possess certain characteristics: the gates are said to offer the OR-facility, to possess OR-ability, or to be OR-able.

Some of the Mullard E^{2}CL gates possess OR-ability; that is, they can be connected to give the OR function of two or more AND or NAND outputs.

As a quite separate feature from the OR-ability just mentioned, some E^{2}CL devices provide within themselves a two level logic output by internal OR-ing. This fact does not necessarily preclude further OR-ing of these devices.

The nature of any two level logic provided by, or available from, any of the E^{2}CL devices is fully explained under the relevant description.

Negative and Positive Logic

Logic gates in digital computers operate with only two signal voltage levels, representing the binary digits 0 and 1. It is necessary, therefore, that when any logic system is considered, a definition of which of these two voltages represents 0, and which voltage represents 1, should be decided at the outset and followed consistently throughout.

Negative Logic is defined, for the purposes of this article, as that system in which the more negative voltage invariably represents 1, and the less negative voltage invariably represents 0.

Positive Logic is defined, for the purposes of this article, as that system in which the more positive voltage invariably represents 1, and the less positive voltage invariably represents 0.

Negative logic has been chosen for use in the literature describing Mullard E^{2}CL devices. The digit 1 or the 'signal present' is therefore indicated by −0·7V at an output, and the digit 0 or 'signal absent' by 0V (ground potential) at an output.

Any decision to employ either one logic system or the other, however, will obviously not affect the electronic action within the logic gate: the hardware operates in the same way whichever convention is used. The function fulfilled by a logic gate therefore depends on the logic definition used. For example, an AND gate with the positive logic definition will give an output of 1 only when all the inputs are at 1, yet the same gate with no electrical changes gives under the definition of negative logic an output of 0 only when all the inputs are at 0 and is therefore an OR gate under this definition. A list of equivalent basic functions under the two definitions is given in Table 2.

TABLE 2

Functions of Logic Gates under Alternative Logic Definitions

Positive Logic	Negative Logic
AND	OR
OR	AND
NAND	NOR
NOR	NAND

The names given to the various Mullard E^{2}CL devices are for negative logic, and therefore the standard E^{2}CL gate is an AND-with-NAND gate. Nevertheless, the Mullard published data usually states in addition that the alternative functions are performed by each device if the logic is re-defined as positive.

Once a logic definition has been stated for a system, it is advisable that this definition should be adhered to without exception throughout the whole system. This point is of importance where E^{2}CL is used in conjunction with another logic system. It is customary, for example, to speak of certain DTL (Diode Transistor Logic) systems as using positive logic: if this system is linked to an E^{2}CL system then either the logic could be redefined as positive for E^{2}CL, and all the E^{2}CL gate functions altered accordingly, or the logic could be redefined as negative for the DTL system and all the DTL gate functions changed accordingly. This question will almost invariably arise when the E^{2}CL interface unit FKL101 (page 170) is used or when E^{2}CL drives directly into DTL, etc., systems.

It is possible, however, to use positive logic for DTL, etc., and continue to use negative logic for E^{2}CL even when they are linked. In general, if this procedure is adopted, an inversion of all logic symbols must be applied on every occasion that signals cross from the negative to positive logic or vice versa: no actual inversion occurs in the electronic gating (see FKL101, page 172), but the reversal of logic definitions demands that all symbols at value 1 become 0 and all at value 0 become 1: inverting every logic symbol at every interface allows for this. It can be seen that the ramifications of adopting this procedure may become numerous and complicated in a large system, particularly when some gates take inputs both from within their own system and also from the other system. Nevertheless, the simultaneous use of both definitions in appropriate areas is possible, if care is taken.

CONCISE DESCRIPTION OF MULLARD E^{2}CL RANGE

It was stated earlier that the initial Mullard range of ten E^{2}CL devices consists of six logic circuits, one line receiving circuit, two staticisors, and an interface unit. The six logic circuits consist of two gates which are not OR-able in any way, three which provide the OR-facility to attain two level logic, and one OR-able line driver. These are mentioned briefly below and are then described more fully in the succeeding pages.

The performance figures given for the devices were obtained from initial development samples.

Dual AND-with-NAND Gate for Single Level Logic (FKH111)

The Mullard FKH111 consists of two AND-with-NAND gates within the same encapsulation: they are independent except for the common power supply rail and an internal voltage reference chain.

Each gate has four inputs, an AND output and a NAND output. Each of the four outputs is terminated within the encapsulation with a 75Ω resistor which cannot be disconnected. (It is for this reason that the gates are not OR-able, in contrast with, for example, FKH101.)

Twin Output Gate (FKH161)

The FKH161 consists of two gate circuits which are not independent. They are commoned in such a way that the outputs of AND-with-NAND for six inputs are simply duplicated. The circuit is a six input gate with two identical pairs of outputs: this is useful for driving two separate lines. Although the two pairs of outputs are logically identical, they are electrically isolated.

Single Line Driver (FKH121)

The FKH121 consists of a single line driver E²CL gate with six inputs. An AND output and a NAND output are provided but have no terminating resistor connected. Four separate 75Ω terminating resistors are provided at other terminals so that the various forms of line driver terminations can be arranged.

Dual Line Receiving Unit (FKH141)

The FKH141 consists of two independent E²CL circuits modified as described on page 165: for each circuit, the pair of inputs must be driven out of phase. Four output terminating resistors are provided at separate terminals for use if required.

Dual AND-with-NAND gate for Two Level Logic (FKH101)

The FKH101 consists of two AND-with-NAND gates within the same encapsulation: they are independent except for the common power supply rail and an internal voltage reference chain. Each gate has three inputs, an AND output and a NAND output. None of the four outputs has a terminating resistor connected, but two 75Ω terminating resistors are provided. Therefore OR-ing between the outputs can be achieved to provide two level logic, or the resistors may be used as termination resistors.

Single 8-input Two Level Logic and Expander Gate (FKH131)

The FKH131 consists of two E²CL gates (each with four inputs) arranged with the outputs OR-ed. There are two output terminals, one of which provides the NAND function (expansion) of all the eight inputs: the other output terminal provides the OR function of the two sets of four AND-ed inputs. The outputs thus give two level logic. The two outputs are not terminated, but two separate 75Ω resistors are provided at other terminals for use if required.

Single 8-input Two Level Logic Unit giving OR-ed AND (FKH171)

This circuit is different from the normal E²CL configuration in many respects, but it is compatible with the E²CL range. The circuit provides internally two AND functions of four inputs; these functions are then OR-ed, and a single unterminated output is provided. A 75Ω terminating resistor is provided at one terminal. The OR-ed AND output can be further OR-ed with other FKH171 outputs. The FKH171 does not itself provide a gating action, and must be used with another E²CL device to provide gating action.

The advantage of using the FKH171 instead of the apparently similar FKH131 is discussed in the section on FKH171.

Interface Unit FKL101

The FKL101 is for use where other logic systems (such as DTL) with a +4V to +6V nominal logic voltage level are required to drive E²CL devices. There are four independent interface circuits within the unit, with common supply voltage rails. Three of the four interface circuits have twin inputs, and the remaining circuit has a single input.

S.R. Clocked Staticisor (FKJ101)

The FKJ101 staticisor has facilities in addition to the staticising function. It has forced Set, forced Reset, Clock and three signal inputs. Two of the signal inputs can be used to vary the logic function. Duplicated AND-with-NAND outputs are provided.

J.K. Flip-flop (FKJ111)

The J.K. flip-flop provides three J inputs which are AND-ed, and three K inputs which are AND-ed. There are also forced Set and Reset inputs and the Clock input. In addition, protection against clock skew is provided.

A normal E²CL AND-with-NAND output is provided, except that the $\bar{Q}$ output has a 75Ω terminating resistor internally connected, whereas the Q output has no resistor connected: a separate 75Ω resistor is provided at another terminal.

Unused Terminals

Input terminals not required for the logic function arranged in any application must be connected to the logical 1, either by connection to a point which is permanently at −0·7V or by connection directly to the negative supply rail.

Output terminals which are not used for driving must be connected, preferably through a 75Ω resistor, to the earth rail. Where a 75Ω resistor is not available in the device, one may be added separately.

DETAILS OF FKH111

The logic function diagram of FKH111 is shown in Fig. 13. The circuit is the normal E²CL gate as described earlier (Fig. 12 on page 157), duplicated to provide two gates which are functionally independent: parts of the voltage reference circuit are not duplicated and are shared by the gates, but this is in no way affects the independent operation of the gates. Each gate has four inputs and the AND-with-NAND outputs are available from each gate. Each of these four outputs has a 75Ω terminating resistor internally connected for termination at the sending end.

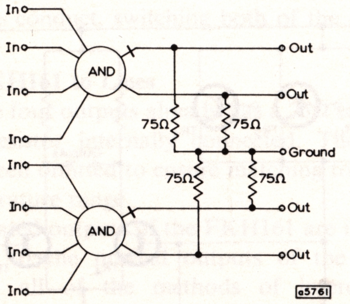

Fig. 13—Logic function of FKH111 for negative logic

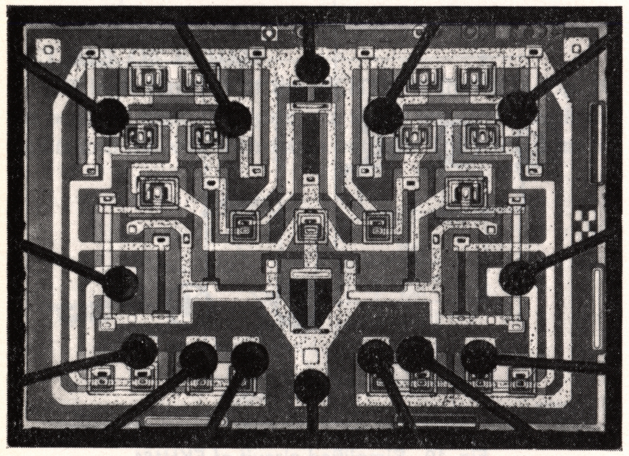

Fig. 14—Development version of the FKH111 integrated circuit chip (approximately 1·75mm long and 1·25mm wide)

A photograph of a Mullard FKH111 chip is shown in Fig. 14. The chip is about 1·75mm long and 1·25mm wide.

Connecting FKH111 to Lines

The FKH111 is primarily intended to be used with short interconnections to succeeding gates: when the total propagation delay in a length of transmission line is short compared with the rise time of the signal then the line appears more as a capacitive short circuit connection than as a transmission line, and need not be treated as a true transmission line. With the rise time of the Mullard E²CL gates, lines of about 3in (8cm) or less fall into this category.

To minimise any deterioration of the rise time, the capacitance of the interconnections should be small, and, in this context, it is permissible to use transmission lines of which the characteristic impedance is higher than the usual 75Ω to obtain a decrease in capacitance. In printed circuitry, this means a reduction of the ratio of width of conductor to thickness of dielectric. It is, however, unadvisable to exceed about 100Ω characteristic impedance or noise pick-up may increase.

The rise time obtained in this configuration depends on the number of gates fanned-out, the length of the spur lines and their characteristic impedance. The results shown in Fig. 15 show rise time and fall time plotted against fan-out for various lengths of 75Ω line. (To make the results in this and the subsequent similar performance graphs easier to read, continuous lines (or 'dotted' lines) are shown linking the rise time values for various fan-out figures: it is clear, however, that fan-out can have only integral values). The deterioration of rise times and fall times in Fig. 15 is mainly caused by the extra capacitance of the longer line lengths, rather than by the loading of gates: all of these times could be improved by about 30% if 100Ω transmission lines were used.

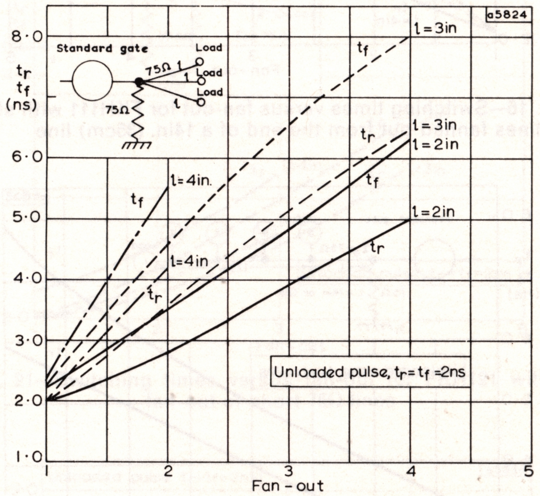

Fig. 15—Switching times versus fan-out for FKH111 with short lines fanned out from the gate

The FKH111 can be used with a longer line, that is, one where the pulse rise time is short compared with the propagation delay in the line: under these conditions each output terminal of the FKH111 should have only one line connected to it. A fan-out may be arranged at the far end of this single line. The performance obtained with this configuration (shown in Fig. 16) is the same as that of the configuration discussed above (Fig. 15). Although line length used for measurements in Fig. 16 was confined to 14in (about 35cm) the only considerations that need limit this length in practice are those of noise pick-up and earth-plane noise, both of which are likely to increase at very long line lengths: a line length of 10in to 14in (about 25cm to 35cm) will be the maximum usable in many environments.

A variation of the previous configuration is shown in

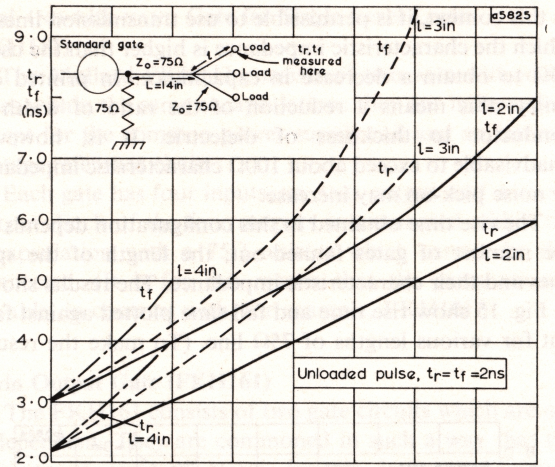

Fig. 16—Switching times versus fan-out for FKH111 with short lines fanned out from the end of a 14in. (35cm) line

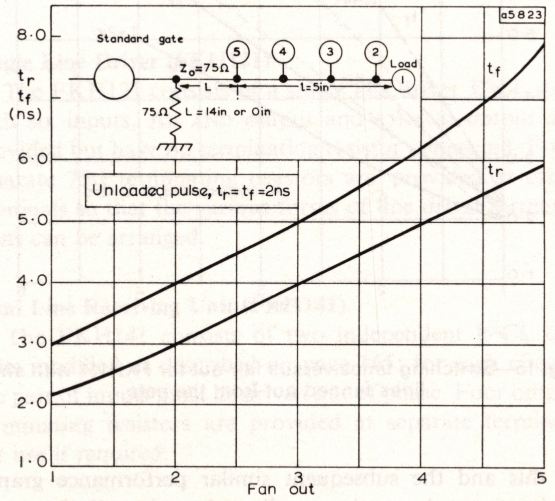

Fig. 17—Switching times versus fan-out for FKH111 with short lines distributed over a short section at the end of 14in. (35cm) of line. The increasing load is added in sequence from the far end

Fig. 17. The fan-out is evenly distributed over 5in (about 12cm). The performance obtained is unaffected by the presence of, or by the length (L) of a section of unloaded line preceding the distributed load: the results shown in Fig. 17 were measured both for L = 0 and for L = 14in (or 35cm) and the results are identical. The value of L is again limited in practice by noise pick-up and ground-plane noise.

The distribution of load in Fig. 17 is even, that is, the space between loads is identical in every case. For a fan-out of one, only gate 1 was connected: for a fan-out of two, only gates 1 and 2 were connected, and so on.

It is necessary to bear in mind with each of the above three configurations, but particularly with that shown in Fig. 17, that initially, only a half pulse travels along the line and that this is doubled during reflection at the high impedance load. For this reason it is advisable to confine the distributed load in Fig. 17 to about 5in (about 8cm): this restriction ensures that the reflection from gate 1 has returned within the rise time of the pulse to gate 5 to give complete switching of gate 5.

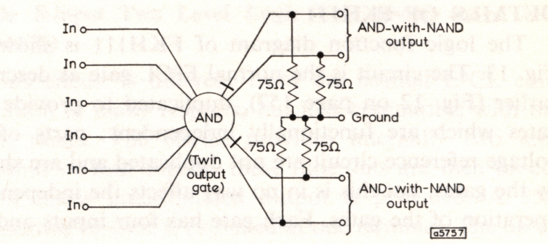

Fig. 18—Logic function ot FKH161 for negative logic

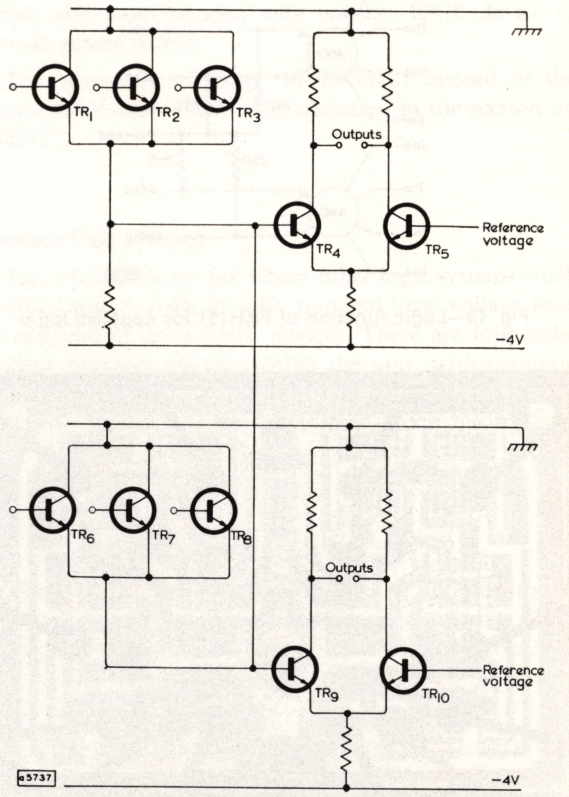

Fig. 19—Simplified circuit of FKH161

If the occasion arises when, in the practical use of the Mullard $\mathrm{E^2CL}$ range, it is necessary to transmit the logic signals over a distance significantly greater than about 14in (35cm), then the FKH111 should preferably not be used. One of the other gates in the range, capable of being used with longer lines, should be used. The FKH101 with far end termination may be considered as one possibility, but for very long lines the FKH121 should be used (perhaps also with the FKH141).

It is also necessary to point out that any form of interconnection essentially different from the three described earlier is unusable with the FKH111 because mismatching and reflection are inevitable: other gates in the series should be chosen for particular applications.

DETAILS OF FKH161

The logic function of the FKH161 is shown in Fig. 18 for negative logic. The gate operates as a single AND-with-NAND gate with a duplicated output. The gate has six inputs, and the two pairs of outputs are electrically isolated but are logically identical.

The circuit consists of two $\mathrm{E^2CL}$ gates, each having three inputs, with an internally connected link between the emitters of the input emitter followers. A simplified form of this circuit is shown in Fig. 19. When any one of the six input signals is 'high' at 0V then the bases of both TR_4 and TR_9 are also 'high' and both of these transistors conduct. When all inputs are 'low' at −0·7V both TR_4 and TR_9 cut off, and the other output transistors TR_5 and TR_{10} conduct, switching both of the outputs.

Connecting FKH161 to Lines

Each of the four outputs already has a 75Ω sending end terminating resistor internally connected. The catching diodes have been omitted to ensure matching to lines over the full temperature range.

The duplicated outputs of the FKH161 are identical in every respect to the normal outputs of the FKH111. Consequently, all of the methods of interconnection described under FKH111 apply to the FKH161. Equally, all the loading rules indicated under FKH111 apply here, as do the performance curves.

DETAILS OF FKH121

The logic function of the FKH121 is shown in Fig. 20 for negative logic. The gate is a single line-driver with six inputs and the AND-with-NAND outputs. The circuit can be considered as being a standard gate (Fig. 12), except that twice the standard current is provided by the long-tail-pair.

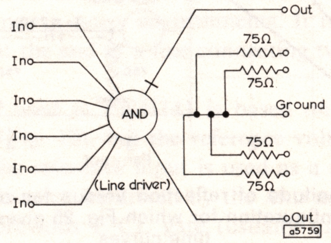

Fig. 20—Logic function of FKH121 for negative logic

Connecting FKH121 to Lines

To provide versatility in the method of driving lines, there are four 75Ω terminating resistors which are not connected to the gate output but are brought out to separate terminals for use as required.

Since the output circuit of the FKH121 provides twice as much current drive as a normal $\mathrm{E^2CL}$ gate, larger fan-out figures may be attained for the same degree of deterioration in rise and fall times, or improved rise and fall times may be attained for similar fan-out figures.

The performance curves shown in Fig. 21 are for the FKH121 using a $37\frac{1}{2}\Omega$ sending end termination and short interconnections of characteristic impedance equal to 75Ω. The use of the low impedance drive compared with FKH111 improves the performance. The same results apply if a $37\frac{1}{2}\Omega$ line is inserted between the termination and the point of fan-out in the same way as was mentioned under FKH111.

The curves shown in Fig. 22 are intended mainly to show the performance with a fan-out of $37\frac{1}{2}\Omega$ lines preceded by an unloaded line of $37\frac{1}{2}\Omega$ impedance. The curves also apply, as argued in the previous paragraphs, to the same configuration where L can have any value including zero. The deterioration in this configuration is caused by the higher capacitance per unit length of the stub lines.

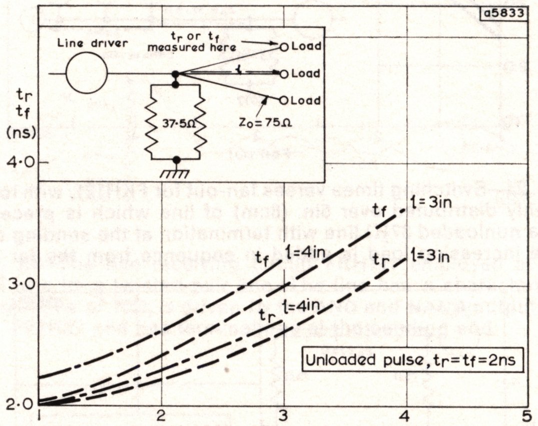

Fig. 21—Switching times versus fan-out for FKH121 with a fan-out of short 75Ω lines

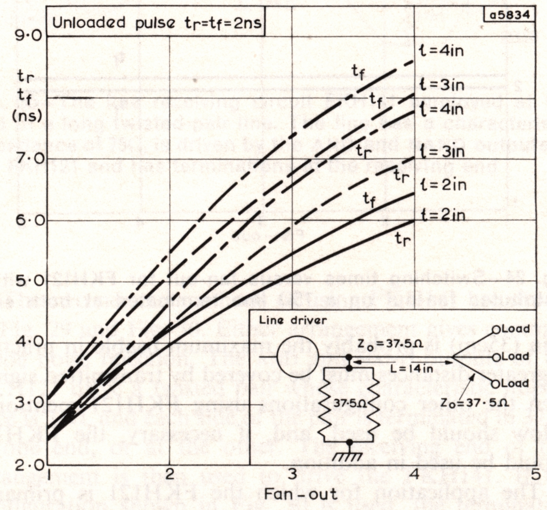

Fig. 22—Switching times versus fan-out for FKH121 with a fan-out of short 75Ω lines preceded by an unloaded $37\frac{1}{2}\Omega$ line with termination at the sending end

The curves shown in Fig. 23 are for a load distributed over 5in (or about 12cm) of $37\frac{1}{2}\Omega$ line, preceded by a length L of $37\frac{1}{2}\Omega$ line. Again, the length of L may take values other than the 14in (or 35cm) chosen, including zero. For a fan-out of one, only gate 1 was connected: for a fan-out of two, only gates 1 and 2 were connected, and so on.

The limitations on the value of L in the above arrangements are imposed by noise pick-up and ground-plane noise, as was mentioned under FKH111. A length of

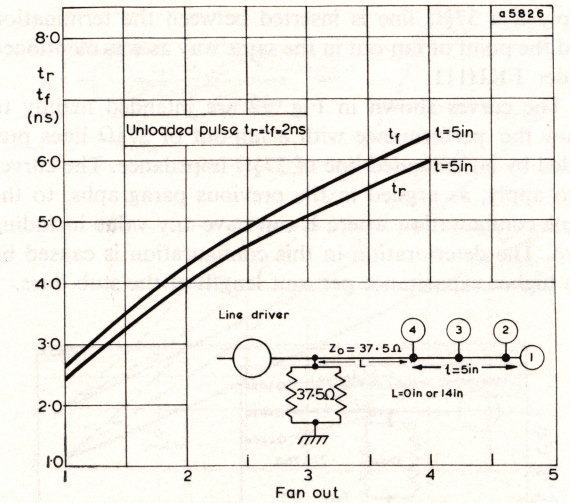

Fig. 23—Switching times verses fan-out for FKH121, with loads evenly distributed over 5in. (8cm) of line which is preceded by a nunloaded 37½Ω line with termination at the sending end. The increasing load is added in sequence from the far end

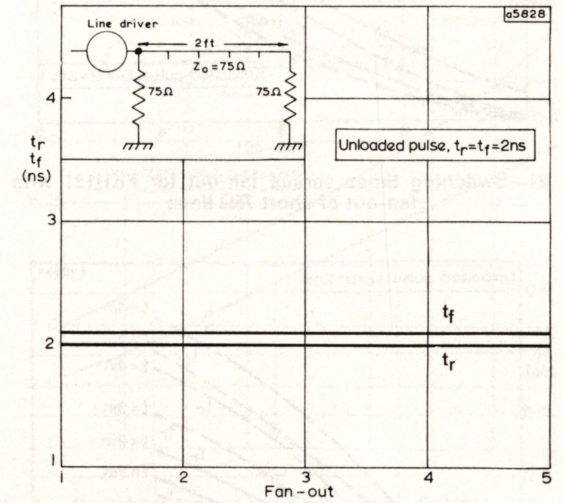

Fig. 24—Switching times versus fan-out for FKH121 with a distributed fan-out on a 75Ω line terminated at both ends

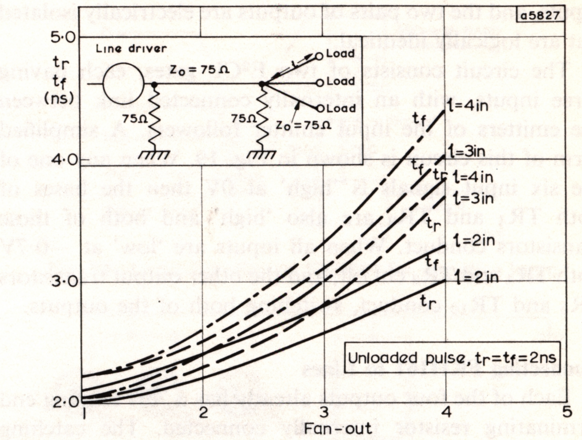

Fig. 25—Switching times versus fan-out for FKH121 with a fan-out of short 75Ω lines at the far end of an unloaded 75Ω line which is terminated at both ends

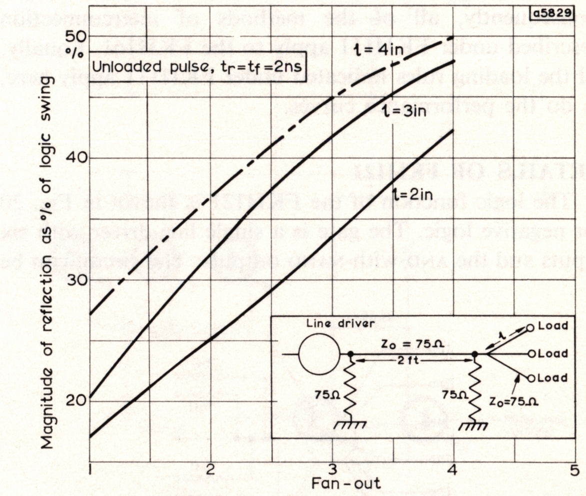

Fig. 26—Magnitude of reflection versus fan-out for FKH121, using the configuration for which Fig. 25 gives the switching time curves

14in (35cm) is probably the maximum usable in practice. If greater distances must be covered by transmitted signals then the other configurations using FKH121 mentioned below should be used, and, if necessary, the FKH141 should be used in addition.

The application for which the FKH121 is primarily intended is to drive a line which is terminated at each end in 75Ω. It is then possible to 'tap-off' receiving gates along the whole length of the line, and the performance curves for this configuration are shown in Fig. 24. There is no significant deterioration of the edge of the pulse, but there is a gradual slowing down of the wave as it progresses along the distributed load: this assumes an evenly distributed load. If the load needs to be somewhat concentrated along part of the line, then the excessive capacitance caused by this can be counterbalanced by using lines of higher impedance along that particular part of the line.

An alternative arrangement using the line terminated at each end is to have the fan-out at the far end, as in Fig 25. (The performance indicated is almost identical with the performance that would be obtained if an unloaded 37½Ω line were placed between the termination and the fan-out in the configuration of Fig. 21; this, in turn, is identical to the performance shown in Fig. 21.)

A combination of distributed load (Fig. 24) and far-end fan-out (Fig. 25) can be arranged, but account must be taken of the inevitable capacitive reflection that occurs from the more concentrated load at the far end: the magnitude of the reflection is shown in Fig. 26. If the operating speed is, in practice, so high that time cannot be allowed for the capacitive reflection to travel back to the sending end and be absorbed, then the far-end fan-out should be restricted as shown in Fig. 27.

The advantage of using the form of line which is terminated at both ends is that the line is less susceptible to noise pick-up and interference. Any disturbance which is picked up is absorbed at one end or the other without further reflections. Any disturbance, therefore, that is picked up requires only one journey along the line before it is absorbed, in contrast to the two journeys some disturbances make in the other configuration.

When termination is required at the far end, this must be provided either by the use of a discrete component or by using a resistor from a package of thin-film resistors. A resistor used in this way must have a tolerance no worse than ±5%, and preferably ±1%.

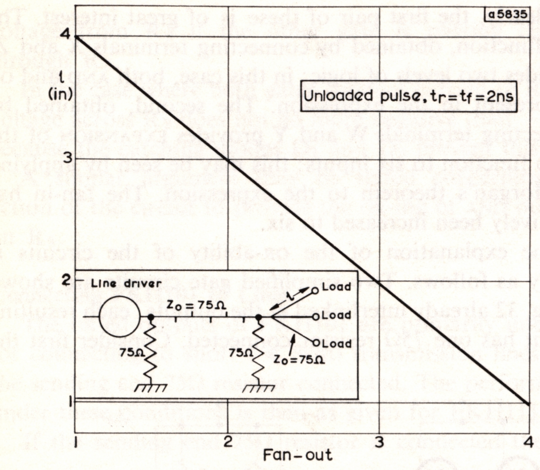

Fig. 27—Permissible length of stub line versus fan-out for FKH121 in the configuration used for Figs. 25 and 26 for high speed operations

DETAILS OF FKH141

The logic function of the FKH141 is indicated in Fig. 28. This circuit is intended solely for use at the receiving end of long lines in noisy environments. It may be used, for example, at the end of a line connecting two boards in a computer.

The circuit used in FKH141 is based on the normal E²CL circuit (Fig. 12), but the reference voltage chain is omitted and the reference input is used as a signal input. The two inputs must be driven by the AND and the NAND output of a previous E²CL gate (usually the FKH121). The effective logic swing is therefore 1·4V instead of 0·7V, as a result of which the noise margin is doubled. Further immunity to noise is derived by common mode noise rejection at the differential input.

The four 75Ω termination resistors are not internally connected, and are brought out at separate terminals.

Connecting FKH141 to Lines

The output of the FKH141 has no resistors internally connected and so each output can be arranged in any of the ways mentioned under FKH111 or FKH101, and the performance is the same. Since, however, the FKH141 is the line receiving unit, the line connection to the input is of greater interest.

The input of the FKH141 must be driven by both the AND and the NAND outputs of a previous gate, and each connection must be appropriately terminated. Clearly, a number of such arrangements driven by other E²CL gates can be devised. In practice, however, only two of these arrangements are of any importance, and these two are entirely adequate for arranging all very long interconnections.

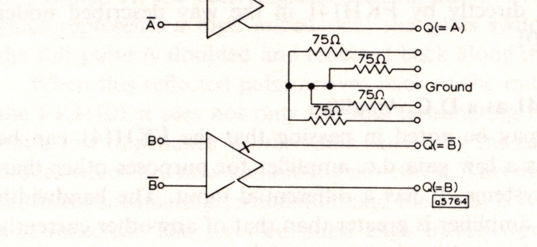

Fig. 28—Logic function of FKH141

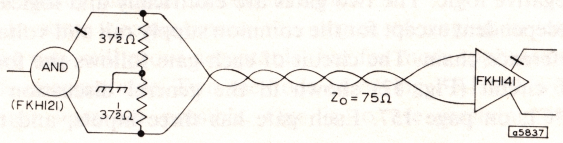

Fig. 29—The line receiving circuit FKH141 employed at the end of a long twisted-pair line. The line has a characteristic impedance of 75Ω, is driven by the AND and NAND outputs of FKH121 and has terminations at the sending end

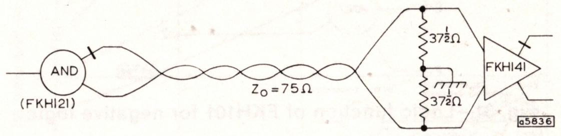

Fig. 30—The line receiving circuit FKH141 employed at the end of a long twisted-pair line. The line has a characteristic impedance of 75Ω, is driven by the AND and NAND outputs of FKH121 and has terminations at the receiving end

The two normal methods of using FKH141 are shown in Fig. 29 and Fig. 30. Either arrangement gives common mode noise rejection. The AND and NAND outputs of the FKH121 drive a twisted pair whose characteristic impedance is 75Ω, and each side of the pair is terminated in 37½Ω at one end, or at the other. The receiving end of this arrangement is then used to drive the FKH141. If the configuration shown in Fig. 30 is used, the terminating resistors may have to be discrete components, or taken from a package of thin-film resistors (see FKH121).

Possible alternative arrangements to those mentioned above include the use of an ordinary E²CL gate such as FKH111 or FKH101 for driving the twisted pair. These, however, demand a twisted pair of 150Ω characteristic impedance: the use of double 75Ω coaxial cable, with the outers grounded at the appropriate end, is not likely to be economical.

OR-ability, and Driving DTL, etc.

The outputs of the FKH141 gates may be OR-ed in the way described under FKH101. Each OR-ed output must have a total of 75Ω d.c. load. DTL, etc., circuits may be driven directly by FKH141 in the way described under FKL101.

FKH141 as a D.C. Amplifier

It may be noted in passing that the FKH141 can be used as a low gain d.c. amplifier for purposes other than logic systems. It has a differential input. The bandwidth of this amplifier is greater than that of any other currently available amplifier in integrated form.

DETAILS OF FKH101

The logic function of FKH101 is indicated in Fig. 31 for negative logic. The two gates are electrically and logically independent except for the common supply rail and voltage reference chain. The circuit of each gate follows the form of circuit (Fig. 12) shown in the general discussion of E²CL on page 157. Each gate has three inputs, and the four outputs have no terminating resistors connected. Two 75Ω resistors are available at other terminals.

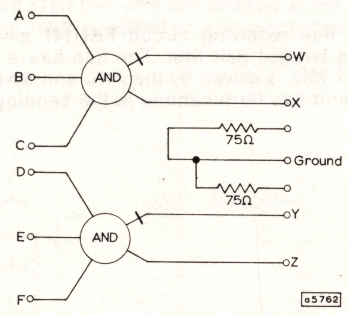

Fig. 31—Logic function of FKH101 for negative logic

Each gate operates as an AND-with-NAND gate for negative logic. This may be written as follows: if signals are applied as in Fig. 31, then

$$f_{(\text{terminal W})} = \overline{A.B.C}$$
$$f_{(\text{terminal X})} = A.B.C$$
$$f_{(\text{terminal Y})} = \overline{D.E.F}$$
$$f_{(\text{terminal Z})} = D.E.F$$

The two gates may be used simply as ordinary AND-with-NAND gates, using any of the termination methods described earlier, provided that it is borne in mind that only two 75Ω resistors are available within this unit.

One of the merits of the FKH101 is that it provides the OR-facility, and, for this, only two resistors are required; OR-ing can be achieved by connecting together two appropriate output terminals, and ensuring that their common output is loaded with only one 75Ω resistor. The outputs that may be derived by this means can be written as follows:

$$f_{(\text{terminals X, Z})} = A.B.C + D.E.F$$
$$f_{(\text{terminals W, Y})} = \overline{A.B.C} + \overline{D.E.F}$$
$$= \overline{A.B.C.D.E.F}$$
$$f_{(\text{terminals W, Z})} = \overline{A.B.C} + D.E.F$$
$$f_{(\text{terminals X, Y})} = A.B.C + \overline{D.E.F}$$

Clearly, the first pair of these is of great interest. The first function, obtained by connecting terminals X and Z, provides two levels of logic; in this case, both AND and OR are present in the expression. The second, obtained by connecting terminals W and Y provides EXPANSION of the NAND function to six inputs: this may be seen by applying de Morgan's theorem to the expression. The fan-in has effectively been increased to six.

The explanation of the OR-ability of the circuits is briefly as follows. Two simplified gate circuits are shown in Fig. 32 already interlinked at the outputs: each resulting output has one 75Ω resistor connected. Consider first the upper gate only. If the bases of both TR_1 and TR_2 receive a 1 signal (−0·7V) then both bases are in the 'low' condition. Therefore the base voltage of TR_3 is also in its 'low' condition and TR_3 is non-conducting. The collector of TR_3 is therefore in the 'high' condition at 0V. If, now, the base voltage of either TR_1 or TR_2 is taken to 0V then the collector of TR_3 goes down to −0·7V. Thus the collector of TR_3 provides the NAND function of the inputs which are applied to TR_1 and TR_2, the output voltage appearing at R_2.

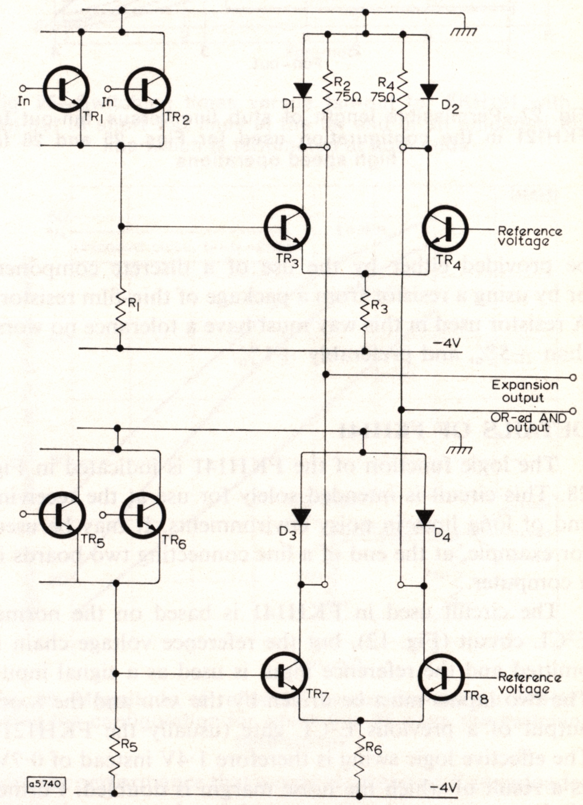

Fig. 32—Simplified FKH101 gate with OR-ing connections made externally

If, however, we consider the lower gate the same action occurs between TR_5 and TR_6 at the input, and R_2 at the output.

The −0·7V 'low' output voltage occurs if either TR_3 or TR_7 is conducting, that is, the overall output at R_2 is an OR-ed NAND function of the inputs. The absence of current into R_2 from one of the gates will not remove the voltage from R_2 if the other gate is passing current through R_2.

In the case where both gates conduct current in R_2 the voltage across R_2 does not go more negative than −0·7V because the catching diodes D_1 and D_3 prevent this.

A similar argument may be stated concerning the action of the circuit to provide the OR-ing of AND outputs on R_4.

Connecting FKH101 to Lines

The OR-ed outputs of FKH101 are primarily intended for connecting to short (⩽ 8cm) transmission lines with the sending end 75Ω resistor connected. The performance under these conditions is then as given for FKH111.

If the sending end 75Ω resistor is connected then no attempt should be made to use longer lines. Longer lines may cause spurious switching of the receiving gate because of 'ringing' in the line. The explanation of this is as follows. On those occasions when both gates drive current into the sending end terminating resistor simultaneously, a full pulse is sent into the line, because the two current outputs see the 75Ω line and the 75Ω resistor in parallel. At the receiving end the fan-out of receiving gates represents a high impedance; the gates switch and the full pulse is doubled and reflected back along the line.

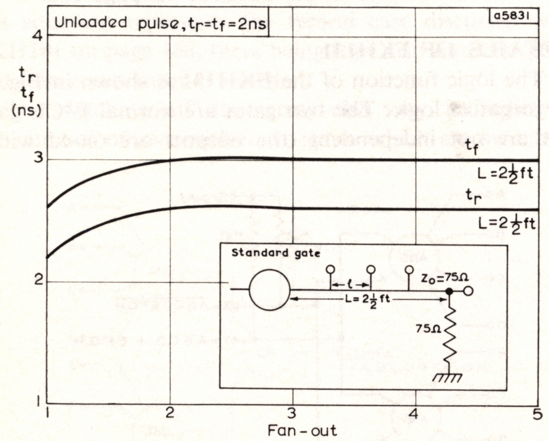

Fig. 33—Switching times versus fan-out for FKH101 with a load evenly distributed along a 75Ω line with termination at the receiving end

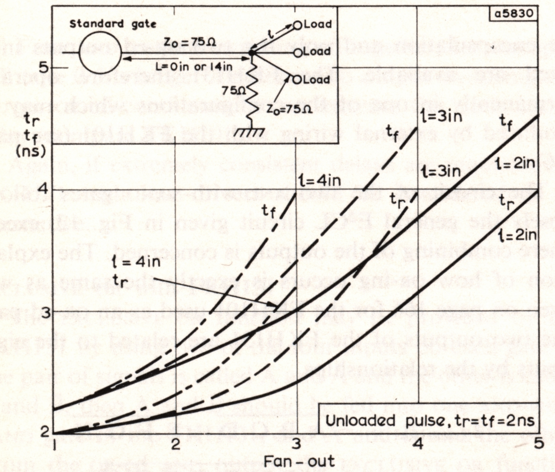

Fig. 34—Switching times versus fan-out for FKH101 with fan-out at the far end and termination at the receiving end of a 75Ω line

When this reflected pulse arrives back at the output of the FKH101 it sees not only the 75Ω terminating resistor but a low impedance to transients caused by the catching diodes which are now conducting at −0·7V. This does not represent satisfactory termination and the pulse is reversed and reflected. The reversed pulse edge travels down the line to the receiving end, and on reaching the receiving gate is doubled and is probably of sufficiently large amplitude to cause the receiving gate to switch back again. After further reflections, the ringing subsides and the receiving gate finally reaches the correct state.

In some circumstances, this degree of ringing in long lines may still prove acceptable, but for most applications it is unacceptable. Two methods of OR-ing FKH101 with longer lines are possible. One is to use receiving end termination. The other is to use the provided sending end termination but add a diode (with 0·7V forward drop) as a discrete component at the receiving end.

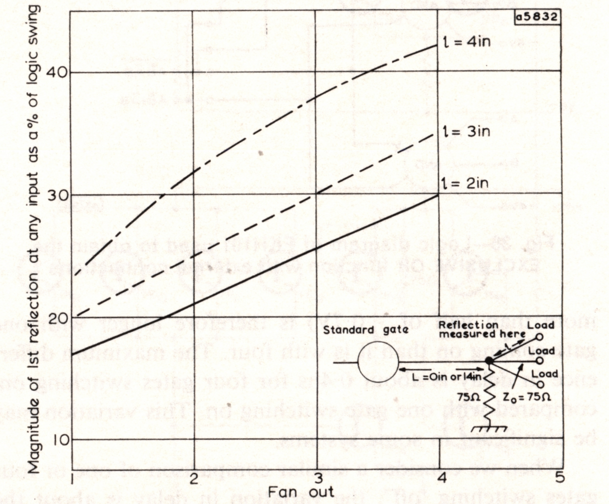

Fig. 35—Magnitude of reflections versus fan-out for FKH101 with the configuration for which Fig. 34 gives the switching times

Since the 75Ω resistors are available but not internally connected in the FKH101, termination of the line can be arranged either at the sending end or at the receiving end.

The performance with an evenly distributed load is shown in Fig. 33. The value of L in the measurements made was 30in (about 75cm) and the value of ℓ was made 6in (about 15cm). For a fan-out of one, only gate 1 was connected: for a fan-out of two, only gates 1 and 2 were connected, and so on.

The performance with a fanned-out load is shown in Fig. 34, and the magnitude of the reflections is indicated in Fig. 35. The magnitude of the reflection can be decreased by increasing the characteristic impedance of the line near the load, as described on pages 153 and 161.

Normally, however, if long lines must be connected to a gate with this kind of logic OR-ability then the FKH101 should not be used: the FKH171 should be used instead, combined with another E²CL gate, probably the line driver FKH121.

Timing of Switching with FKH101

For some design techniques it is essential to know not only the propagation delay of any device, but also the tolerance on this delay. The FKH101 has a slight variability in switching time, which may affect its use in some extremely fast systems if extensive OR-ing is used. If we consider a typical case where two FKH101 units are used, there may be four gates OR-ed to one terminating resistor. When switching 'on' to −0·7V occurs the output transistors have to charge the relevant capacitances of the gate and the associated circuitry. The charging current will be four times as high if all four output transistors switch 'on' at the same time, as it would be for only one output transistor switching on. The time taken to reach the required switching voltage of a succeeding gate (which is slightly more than half of −0·7V) is therefore longer with one gate coming on than it is with four. The maximum difference in delay is about 0·4ns for four gates switching on, compared with one gate switching on. This variation may be significant in some systems.

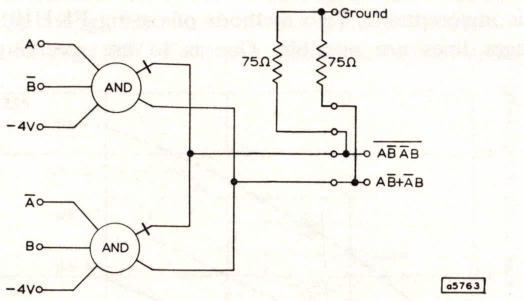

Fig. 36—Logic diagram of FKH101 used to obtain the EXCLUSIVE OR function with external connections

When we consider a similar comparison of one or four gates switching 'off', the variation in delay is about the same, and may again be significant in some applications. If three of the output transistors are non-conducting and the remaining transistor is switched off, then the current in the terminating resistor begins to fall almost instantaneously: this is because almost the entire current of the transistor is carried by the resistor, and the current in the catching diode is negligible. When, for comparison, four gates switch 'off' three of the transistor currents have been conducted through the catching diodes. These diode currents all have to decrease to zero before the voltage can begin to fall from −0·7V. There is therefore a delay (in addition to the normal propagation delay) after the input switches, and this amounts to approximately 0·5ns for four gates switching off. The exact value of delay varies with the number of gates switching off, but it is this variability, rather than the fact of a delay itself, that militates against the use of extensive OR-ing at high clock speeds with the FKH101.

Again, if this problem arises, it may be circumvented by the use of FKH171 instead of FKH101.

EXCLUSIVE OR with FKH101

The EXCLUSIVE OR function may be provided by the FKH101. If the complementary outputs taken from a previous gate are called A and Ā, and the complementary outputs from a second gate are called B and B̄, these should be connected to the FKH101 so that the A and B̄ drive one AND-with-NAND gate in the FKH101, and the Ā and B drive the other gate in the FKH101 (see Fig. 36). From the OR-ed AND of the FKH101 the output is therefore $A.\bar{B} + \bar{A}.B$ which is the EXCLUSIVE OR function of A and B. (For EXCLUSIVE OR, the INVERTED outputs of the FKH101 should be connected together and to one terminating resistor; this output remains at −0·7V. The unused input terminals should be connected to the −4V supply rail.)

Driving DTL, etc., with FKH101

The FKH101 may be used to drive directly DTL and other similar logic circuits. The way in which this is achieved is described under FKL101 on page 170.

DETAILS OF FKH131

The logic function of the FKH131 is shown in Fig. 37 for negative logic. The two gates are normal E²CL gates but are not independent: the outputs are OR-ed within the encapsulation and only the two OR-ed outputs indicated are available. The FKH131 therefore operates permanently in one of the configurations which may be produced by external wiring with the FKH101 (see page 166).

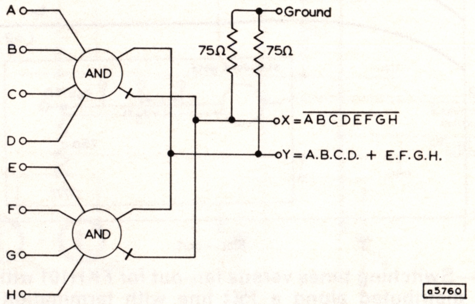

Fig. 37—Logic function of FKH131 for negative logic

The circuit of the two AND-with-NAND gates follows closely the general E²CL circuit given in Fig. 12, except where combining of the outputs is concerned. The explanation of how OR-ing occurs is exactly the same as was given on page 166 for the FKH101 used as an OR-ed pair. The two outputs of the FKH131 are related to the eight inputs by the relationships

$$f_{(\text{terminal X})} = \overline{A.B.C.D} + \overline{E.F.G.H}$$

$$= \overline{A.B.C.D.E.F.G.H}$$

$$f_{(\text{terminal Y})} = A.B.C.D + E.F.G.H$$

Terminal Y thus provides the OR-ed AND function, while terminal X provides the EXPANDED NAND of the inputs.

The main uses for which the FKH131 is intended are, first, to provide a fan-in of eight where this is required, and secondly to provide the OR-ed AND function of two sets of four inputs. Two terminating resistors are available at other terminals.

Connecting FKH131 to Lines

The FKH131 must be used with short transmission lines. The reason for this is precisely the same as given for the FKH101 on page 167. Since, with the FKH131, however, the terminating resistors are permanently internally connected at the sending end, there is no possibility of using receiving end termination. The use of a separate discrete component diode with a forward drop of 0·7V (as mentioned with the FKH101) is still, however, possible.

If the OR-ed AND function is required with longer lines, then the FKH171 should be used with line drivers.

Timing of Switching with FKH131

The switching 'on' times of the FKH131 may vary by 0·4ns if two FKH131 gates are OR-ed with each other: this situation represents the typical case discussed with FKH101 on page 168, there being four AND outputs OR-ed and four NAND outputs OR-ed.

The switching 'off' times may also vary, according to the number of AND-with-NAND gates which are switching off. Four AND outputs switching off together, for example, will take 0·5ns longer than one AND output switching off. Larger OR-ed combinations can increase this variation in delay (compare FKH101).

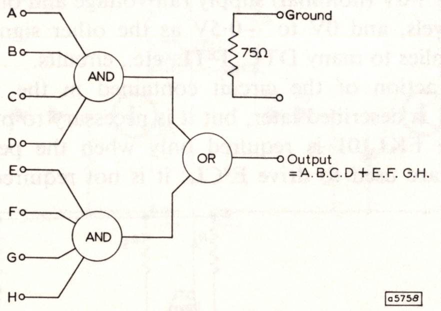

Fig. 38—Logic function of FKH171 for negative logic

Again, if extremely consistent delays are required, the FKH171 with line drivers should be considered as an alternative.

EXCLUSIVE OR with FKH131

The EXCLUSIVE OR function may be provided by the FKH131 by using two of the four inputs on each gate. If one pair of signals is called A and Ā and the other is called B and B̄, then A and B̄ should be fed into one AND-with-NAND gate of the FKH131, and Ā and B into the other. From the OR-ed AND output the EXCLUSIVE OR function $A.\bar{B} + \bar{A}.B$ is provided. In this situation, the EXPANDED output and the remaining input terminals are not used. This situation is almost identical with that for obtaining EXCLUSIVE OR with FKH101, and the unused terminals should be treated in the way mentioned there.

DETAILS OF FKH171

The FKH171 has been provided specifically to overcome the difficulties of variability in switching times, under different conditions of OR-ing, that occur with FKH101 and FKH131. The circuit itself, however, is not a gate; that is, it has no regenerative action. It is a linear device, and is always used in conjunction with one of the E²CL logic gates to provide gating action. The difficulty of reflections when OR-ed outputs drive long lines with FKH101 and FKH131 can also be avoided by using FKH171 with a gate.

The FKH171 performs, for negative logic, the logic function that is shown in Fig. 38, that is, it performs the OR-ed AND operation for two sets of four inputs. There is no alternative output. Therefore the entire logic function of the FKH171 is exactly the same as the logic function for the OR-ed AND output terminal of the FKH131, indicated at terminal Y in Fig. 37. Although the FKH171 may therefore, at first sight, appear less versatile and perhaps redundant, it offers one distinct advantage when very high clock speeds are used: that is, the propagation delay for the FKH171 is consistent whether one, or four, or even more AND gates which are OR-ed, switch to the 'on' or 'off' state. This contrasts with the slightly variable delay in similar circumstances in both FKH101 and FKH131.

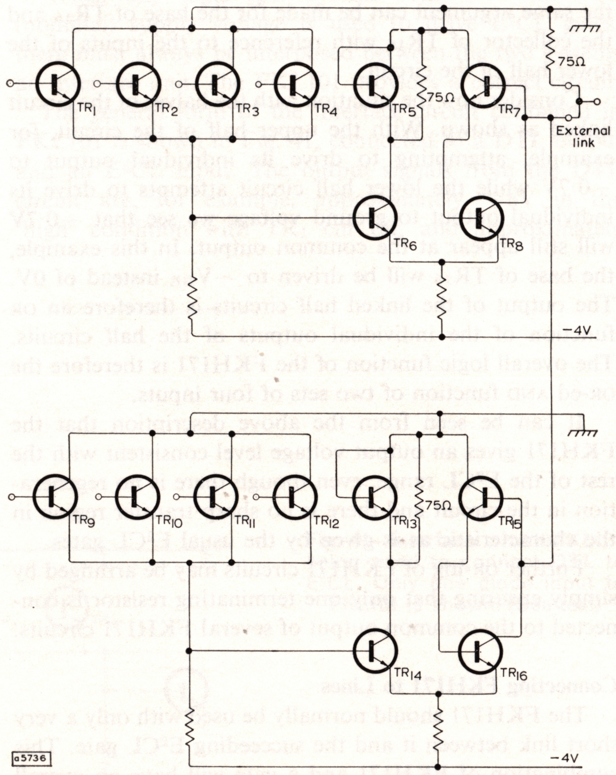

Fig. 39—Simplified circuit of FKH171

A very simplified form of the FKH171 circuit is shown in Fig. 39, and the action of the circuit may be stated as follows. Consider the upper half of the circuit as though it were isolated from the lower half in Fig. 39. If all the inputs to the bases of TR_1, TR_2, TR_3 and TR_4 are at logic level 1, that is −0·7V, their emitters, and the base of TR_6 are therefore 'low' at $-(0{\cdot}7V+V_{BE})$. The emitters of TR_6 and TR_8 are therefore at $-(0{\cdot}7V+2V_{BE})$; from this voltage level the collector of TR_8 and the base of TR_7 will be $2V_{BE}$ higher, and will therefore be at −0·7V with respect to ground. If, now, any one of the base voltages of TR_1, TR_2, TR_3 or TR_4 goes to the 'high' logic level at ground potential, then the emitter of that transistor (say, TR_1) is at $-V_{BE}$ and the base of TR_6 will follow this to $-V_{BE}$. The emitters of TR_6 and TR_8 will therefore now be at $-2V_{BE}$: from this level of $-2V_{BE}$ the base of TR_7 and the collector of TR_8 will be $2V_{BE}$ higher and will therefore be at ground potential.

For the upper half of the circuit alone we may say that the base of TR_7 and the collector of TR_8 provide an AND function of the four inputs, for negative logic. Precisely the same argument can be made for the base of TR_{15} and the collector of TR_{16} with reference to the inputs of the lower half of the circuit.

Consider now the situation with the halves of the circuit linked as shown. With the upper half of the circuit, for example, attempting to drive its individual output to $-0{\cdot}7$V while the lower half circuit attempts to drive its individual output to ground voltage we see that $-0{\cdot}7$V will still appear at the common output. In this example, the base of TR_{15} will be driven to $-V_{BE}$ instead of 0V. The output of the linked half circuits is therefore an OR function of the individual outputs of the half circuits. The overall logic function of the FKH171 is therefore the OR-ed AND function of two sets of four inputs.

It can be seen from the above description that the FKH171 gives an output voltage level consistent with the rest of the E^{2}CL range, even though there is no regeneration in the circuit and there is no sharp transfer region in the characteristic as is given by the usual E^{2}CL gates.

Further OR-ing of FKH171 circuits may be arranged by simply ensuring that only one terminating resistor is connected to the common output of several FKH171 circuits.

Connecting FKH171 to Lines

The FKH171 should normally be used with only a very short link between it and the succeeding E^{2}CL gate. This combination of FKH171 and a gate will have an overall propagation delay of only slightly more than the delay for a single E^{2}CL gate. In addition, the OR-ing will have been obtained, as previously described, without difficulties of variation in timing and without problems of reflection. The E^{2}CL gate used to follow the FKH171 may then drive any length of line that is suitable for it with whatever line termination is adopted.

If long lines are introduced between the FKH171 and the succeeding E^{2}CL gate, spurious switching of the receiving gate may arise under certain conditions of OR-ing in a way similar to that described under FKH101 and FKH131. Thus, if long lines are required with the FKH171, this should be achieved by allowing the FKH171 to drive a line driver (FKH121) after only a very short link and then placing the long line on the output of the line driver.

Timing of Switching with FKH171

There is no significant variability in the delay in either switching 'on' or 'off' with the FKH171, whether the number of AND circuits switching on and off is small or large. This contrasts with FKH101 and FKH131, and for this reason the FKH171 should always be used in high clock speed systems for the OR-ed AND function.

The main reason that little variation occurs in the delay in the FKH171 is that the output of this device is voltage controlled, in contrast to the current controlled outputs of FKH101 and FKH131. Therefore, if more than one AND circuit in the FKH171 switches 'on' then the current through the output resistor is shared by the relevant circuits. Thus, the current available for charging and discharging the load capacitance is almost constant under the various OR-ing conditions.

EXCLUSIVE OR with FKH171

The EXCLUSIVE OR function is obtainable with the FKH171 in a similar way to that described under FKH101 and FKH131.

DETAILS OF INTERFACE UNIT FKL101

The term 'interface unit' may be used to describe any circuit which is used purely for connective purposes between computer subsystems where one is constructed from a different kind of logic gates from those in the other. In particular, an interface unit is required to drive E^{2}CL equipment from a system of peripheral logic gates using $+4$V to $+6$V (nominal) supply rail voltage and one of the logic levels, and 0V to $+0{\cdot}5$V as the other signal level. This applies to many DTL, T^{2}TL, etc., circuits.

The action of the circuit contained in the Mullard FKL101 is described later, but it is necessary to point out that the FKL101 is required only when the peripheral circuits are used to drive E^{2}CL: it is not required in the opposite process where E^{2}CL drives peripheral circuits. Any E^{2}CL gate may drive directly into these peripheral circuits with the conditions that the terminating resistor is not connected and a catching diode is present on the output. This process is discussed first, before the interface unit is described.

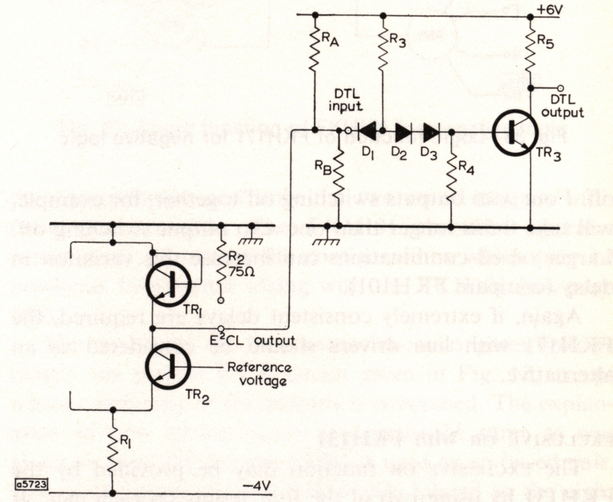

Fig. 40—Simplified E^{2}CL circuit driving directly into DTL. The catching diode in the E^{2}CL circuit must be present, and the 75Ω termination resistor must be disconnected. (See text)

E^{2}CL Driving Peripheral Circuits

In a simplified form, the AND or NAND output of an E^{2}CL circuit is shown in Fig. 40 connected to a DTL input circuit of the kind that appears, for example, in the Mullard FC range of DTL gates. The terminating resistor for the E^{2}CL gate is (and must always be) disconnected. The action of this arrangement is explained briefly as follows.

When E^{2}CL output is 'low' at $-0{\cdot}7$V, the current flows through R_3 and D_1, and thence through TR_2 in the E^{2}CL gate. Since the output voltage of the E^{2}CL gate is caught by the catching diode at $-0{\cdot}75$V, the potential on the anode of D_1 will be the V_{BE} of D_1 higher than $-0{\cdot}75$V, that is it will be approximately at ground potential. The diodes D_2 and D_3 therefore do not conduct and the base of TR_3 receives the 'low' signal in exactly the same way as it would when driven from another DTL gate.

When the E^{2}CL output is 'high' then both TR_1 and TR_2 present a very high resistance path to current from R_3 and D_1. Consequently, the voltage at the output of the E^{2}CL is made positive with respect to ground, by the DTL input circuit because current flows through R_3, D_2, D_3, etc., raising the potential at the point between R_3 and D_2 to about $2{\cdot}1$V with respect to ground. The input to the DTL gate is therefore an ordinary 'high' input corresponding with the E^{2}CL 'high' output. The positive voltage caused at the output of the E^{2}CL gate has no ill effects provided that the voltage appearing at the anode of D_1 is not more than $+5{\cdot}5$V.

The two resistors marked R_A and R_B perform no part in the logic action of this arrangement but may be added to the circuit. The resistor R_A (about 2kΩ) can be included to improve the noise margin of this configuration: the DTL input terminal rises to a more positive voltage than it would in the absence of R_A, and so the noise margin for negative noise is improved. The resistor R_B can be included if necessary to limit the peak positive excursion of the DTL input terminal to $+5{\cdot}5$V to meet the requirements of the E^{2}CL output point: this may not be required with some DTL, etc., circuits.

The explanation given above for driving a DTL circuit is almost unchanged for explaining the driving of TTL and other gate systems. There is no $+4$V to $+6$V logic system known at present which is incapable of being driven by an E^{2}CL output in this way.

The E^{2}CL terminating resistor must be left disconnected: otherwise the DTL input is held in the 'low' position permanently. The gate must also be provided with a catching diode at the output. It is possible therefore to drive $+4$V to $+6$V DTL, etc., circuits from the FKH101, FKH131 and the FKH141.

Peripheral Circuits Driving E^{2}CL with FKL101

When any logic gate system with $+4$V to $+6$V (nominal) supply voltage is used to drive E^{2}CL gates, there must always be interposed between the two systems an interface unit. The FKL101 provides a correct circuit.

The general form of the interface circuit contained in FKL101 is shown in Fig. 41, connected to a DTL output and an E^{2}CL input. The output signals from the DTL circuit are, for example, approximately $+6$V in the 'high' condition with TR_1 cut off, and approximately $+0{\cdot}3$V in the 'low' condition when TR_1 is saturated. The explanation of the action of the interface circuit is briefly as follows.

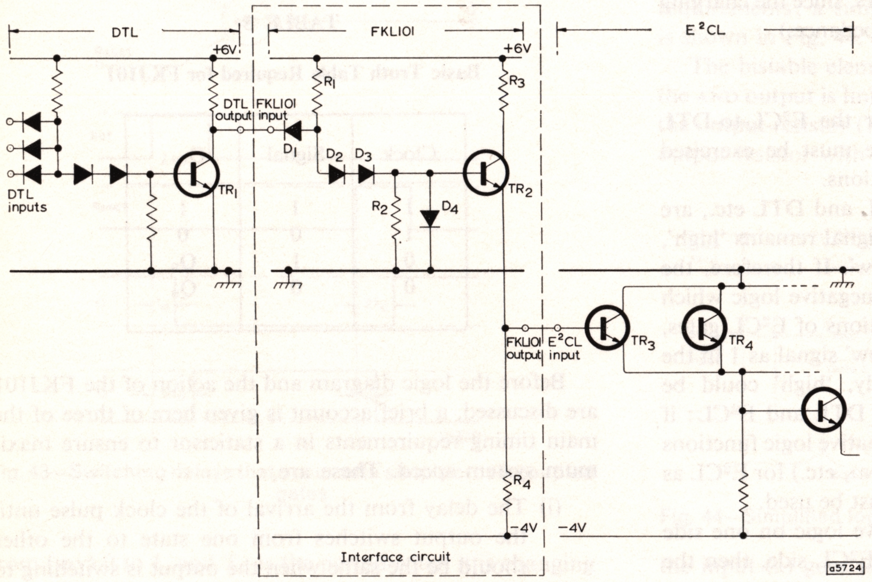

Fig. 41—Interface circuit FKL101 being used to connect DTL to E^{2}CL. Only one diode input to FKL101 is shown. (See text)

When DTL output from TR_1 is in the 'high' condition at $+6$V, the diode D_1 in the interface circuit is cut off. Current is conducted through R_1, D_2, D_3 and R_2 in parallel with D_4; the potential at the base of TR_2 is defined as V_{BE} above ground potential by the diode D_4. The emitter voltage of TR_2 is one V_{BE} down from this value and is therefore approximately at 0V, or ground potential. The output of the interface circuit is therefore 0V when its input is 'high' at $+6$V, and this gives the correct 'high' voltage input to the E^{2}CL circuit.

When the DTL output from TR_1 is in the 'low' position at approximately $+0{\cdot}3$V, the diode D_1 conducts from R_1 into TR_1. The potential at the junction of R_1, D_1 and D_2 is therefore $+0{\cdot}3\text{V}+V_{BE}$, or approximately $+1$V. The two diodes D_2 and D_3 cannot therefore conduct; they would require a total of $2V_{BE}$ or $1{\cdot}4$V for this, and so the base voltage of TR_2 would need to fall to at least $-0{\cdot}4$V.

When the base voltage of TR_2 falls, it is caught at about $-0{\cdot}05$V by the voltage which is caused by base current beginning to flow through R_2. The base current (I_c/h_{FE}) multiplied by the value of R_2 fixes the base voltage at about $-0{\cdot}05$V. Therefore, the emitter voltage of TR_2 is $-V_{BE}$ from this value or approximately $-0{\cdot}8$V. Again, therefore, the output from the interface circuit is at the correct voltage and in the correct sense to drive the E^{2}CL circuit: a DTL 'low' output of $+0{\cdot}3$V has been converted to a suitable 'low' E^{2}CL input of $-0{\cdot}8$V.

Various parameters of this circuit are chosen so that the value of R_2 may be as low as possible, consistent with the correct operation of the rest of the circuit. The reason for this is that when TR_2 is switched from the 'high' condition to the 'low' condition the circuit capacitance at the base of TR_2 must discharge, and D_3, D_4 and TR_2 present only high resistance current paths. The discharge is therefore speeded up by the presence of R_2. This enables switching off to occur at an appropriate speed to minimise the overall delay of the FKL101. (This problem does not arise when switching on occurs, since the charging current is supplied through a low impedance.)

Positive and Negative Logic

The use of either the FKL101 or the E^{2}CL-to-DTL interface connection means that care must be exercised in the choice and use of logic definitions.

It has been shown that when E^{2}CL and DTL etc., are linked in either direction, the 'high' signal remains 'high', and that the 'low' signal remains 'low'. If therefore, the 'low' signal is defined as 1, as in the negative logic which is now customarily used with descriptions of E^{2}CL gates, then one possibility is to define the 'low' signal as 1 in the DTL, etc., system also. Alternatively, 'high' could be defined as 1 (positive logic) for both DTL and E^{2}CL: if this latter option is used then the alternative logic functions (OR-with-NOR instead of AND-with-NAND, etc.) for E^{2}CL as given in the relevant Mullard data must be used.

If a decision is made to use positive logic on one side of the interface and negative on the E^{2}CL side, then the designer must allow for all of the numerous consequences of this arrangement. Every logic symbol that passes the interface must be inverted. The circuit does not, in fact, invert the signal, but the exchange of logic definitions demands that all symbols at value 1 become 0 and all symbols at value 0 become 1 at every interface. Thus an inversion applied to all logic symbols at every interface allows for this.

Logic Function of FKL101

In the FKL101 unit there are four logically independent circuits. One of these has only one input but the other three have duplicated diode inputs.

Those interface circuits with only one input act as voltage level shifters and perform no logic function.

Those interface circuits that have two diode inputs provide a 'low' ($-0{\cdot}7$V) output if either of the inputs is made 'low' (about 0V) and give a 'high' output (0V) only if both of the inputs are 'high' (about $+4$V to $+6$V). Thus if negative logic is applied to both sides of the interface, the circuits perform the OR function between the two inputs; if positive logic is used, the unit performs the AND function between the two inputs. If the logic is to be defined as positive within the DTL system and negative within the E^{2}CL system then the FKL101 circuits with twin inputs may be treated as follows. The interface circuits with twin inputs perform the AND function in the positive logic; the inverse of the logic signal derived at the output of the interface circuit is then employed as the input to the E^{2}CL circuit.

DETAILS OF FKJ101

The FKJ101 is a clocked set-reset staticisor which has been designed for re-clocking and staticising information at a speed consistent with that of the other E^{2}CL devices. The truth table (Table 3) indicates that the staticisor output Q_{n+1} is set to the appropriate value by the input signal during the clock pulse, and that no further change of output occurs between clock pulses even if the input signal changes.

TABLE 3

Basic Truth Table Required for FKJ101

Clock	Signal	Q_{n+1}
1	1	1
1	0	0
0	1	Q_n
0	0	Q_n

Before the logic diagram and the action of the FKJ101 are discussed, a brief account is given here of three of the main timing requirements in a staticisor to ensure maximum system speed. These are,

(i) The delay from the arrival of the clock pulse until the output switches from one state to the other should be the same when the output is switching to 1 as when it is switching to 0.

(ii) The delays mentioned in (i) should both be as short as possible.

(iii) The latch-time of the bistable element in the staticisor should be as short as possible, to allow clock pulses of short duration. (The clock rate attainable will depend on the clock pulse duration, and this depends on the latch time.)

It is necessary to design for each of these three criteria simultaneously to enable high speed clocking to operate successfully. The pulses in Fig. 42 show the delay times which have been mentioned. To satisfy condition (i), t_1 must be equal to t'_1. To satisfy condition (ii), both t_1 and t'_1 must be short. To satisfy condition (iii), the latch time of the staticisor which determines the minimum clock pulse duration t_c must also be short.

The necessity to fulfil condition (i), that t_1 must equal t'_1, is explained as follows. If the time T_1 is defined as the time required for the output to appear, after the beginning of the clock pulse, when the output is changing from (say) 0 to 1, and T_2 is the period when it is changing from 1 to 0, then the following two equations indicate the nominal and variable parts of these two times.

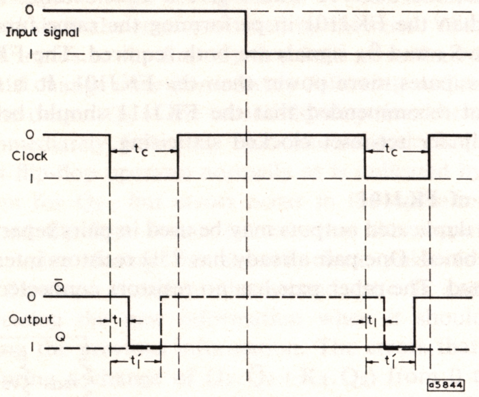

Fig. 42—Switching delays that can occur in some forms of staticisor

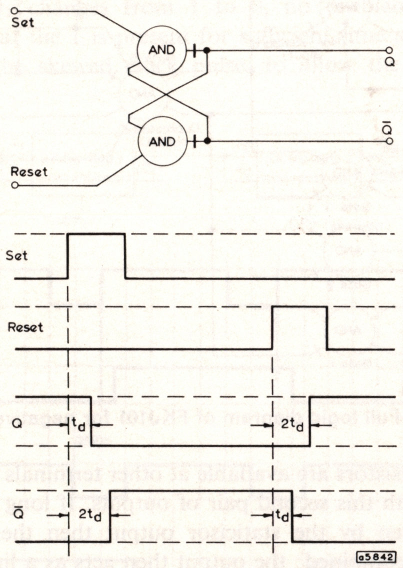

Fig. 43—Switching delays that occur with simple cross-coupled gates

$$T_1 = t_1 \pm \Delta t_1$$
$$T_2 = t'_1 \pm \Delta t'_1$$

The excess time that must be allowed for the bistable element to change state is then given by

$$\Delta T = T_2 - T_1 = (t_1 - t'_1) + \Delta t_1 + \Delta t'_1\,,$$

where the last two terms are device-to-device spreads in delays. If, however, t_1 is made equal to t'_1 (condition (i)) even if this means increasing t'_1, then,

$$\Delta T = \Delta t_1 + \Delta t'_1.$$

This represents a reduction in the value of ΔT, giving a higher system speed.

Since the value of $(t_1 - t'_1)$ in some forms of staticisor can equal one or two stage delays, the saving in time is considerable if condition (i) is satisfied. (A corollary of this is that, in practice, there must also be no significant delay between the switching of Q and $\bar{Q}$; this condition is, however, comparatively easily met within the E^{2}CL output circuits. This will be seen in the logic diagram for FKJ101.)

If there were a comparatively long delay between the arrival of the clock pulse and the changing of the output (t_1 and t'_1) then the clock rate would have to be slowed down to allow for this. Thus, if condition (ii) is not met by the staticisor, then the advantage of using fast gates in the remainder of the circuit may be entirely lost.

Similarly, since the clock pulse duration must always be long enough to allow time for the staticisor to latch, then the latch time must be short to permit short clock pulses and high clock rates. Thus, if condition (iii) is not met by the staticisor, then the advantage of using fast gates is again lost.

From the above reasons it can be seen that a simple staticisor consisting of two cross-coupled gates as shown in Fig. 43 would not satisfy condition (i). It would also require additional gating to fulfil the requirements of the truth table shown in Table 3.

The FKJ101 has been designed to meet all of the above requirements; a simplified logic diagram of the staticisor is shown in Fig. 44.

The bistable element in this circuit is Gate 4, in which the AND output is linked with one of the inputs of the gate: the output resistor (75Ω) of Gate 4 is shared as a common output resistor with Gate 3. The bistable is set to 0 when the input (a) goes to 0, or is set to 1 when both (a) and (b) go to 1. The previous setting is retained while (a) is at 1 and there is not a 1 provided at (b) by Gate 3. (The condition that (a) = 0 and (b) = 1 simultaneously is restrained from occurring by the circuit design.)

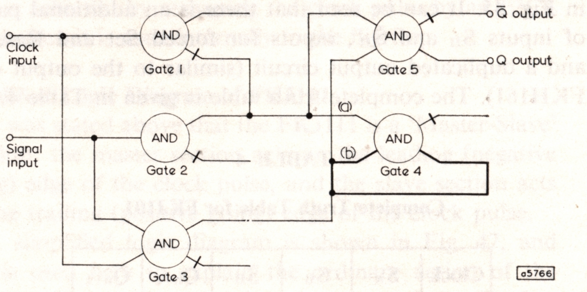

Fig. 44—Simplified logic diagram of FKJ101 for negative logic

The action of the FKJ101 is therefore as follows. When the clock pulse is 1 (present), the inverted output of Gate 1 is always 0; the non-inverted output of Gate 2 is 0 if the signal is 0, and 1 if the signal is 1. Therefore the OR-ed output of Gates 1 and 2 drives Gate 4 with the signal value during the clock pulse. In addition, the non-inverted output of Gate 3 repeats the signal during the clock pulse. During the clock pulse, therefore, Gate 4 is driven by two inputs at 1 if the signal is 1, or two inputs at 0 if the signal is 0. It is therefore set appropriately during the clock pulse. Gate 5 is driven by the same inputs as drive Gate 4 and so the output of Gate 5 indicates the setting of Gate 4.

When the clock pulse is 0 (absent) the inverted output of Gate 1 is always 1, and so the OR-ed output of Gates 1 and 2 drives both Gates 4 and 5 with a 1 between clock pulses. Gate 3 does not provide a 1 output during the absence of the clock pulse despite signal value changes.

Under these conditions (no clock pulse) the previous setting of Gate 4, and the output, Gate 5, remain unchanged.

The logic of the FKJ101 has been arranged to meet the timing requirements specified earlier.

Gate 5 ensures that the Q and $\bar{Q}$ outputs change simultaneously. (If outputs had been taken directly from Gate 4, the outputs would not have changed simultaneously.)

The number of stage delays required for the signal to switch from 0 to 1 is the same as that required for switching from 1 to 0. In addition, the loading of the gates in the signal path is the same in both cases. The total delay in each case is two stage delays plus approximately 0·5ns caused by OR-ing. The latch time for the circuit is two stage delays, and clock pulses should not therefore be shorter than about 5ns.

The only restriction that must be imposed on this circuit is that the signal must not be allowed to change during the clock pulse period.

A further feature of this circuit is that Gate 5 acts as a buffer between the output line and the bistable element. Any disturbance or reflections on the output line cannot destroy the information stored in the staticisor, and the latch time is unaffected by the length of line being driven: this feature can be of major importance in very fast systems.

The complete logic diagram of the FKJ101 is shown in Fig. 45. It can be seen that there is an additional pair of inputs S_B and $\bar{S}_B$, inputs for forced Set and Reset, and a duplicated output circuit (similar to the output of FKH161). The complete truth table is given in Table 4.

TABLE 4

Complete Truth Table for FKJ101

Clock	S_A	S_B	$\bar{S}_B$	Q_{n+1}	$\bar{Q}_{n+1}$
0	1	1	0	Q_n	$\bar{Q}_n$
0	1	0	1	Q_n	$\bar{Q}_n$
0	0	1	0	Q_n	$\bar{Q}_n$
0	0	0	1	Q_n	$\bar{Q}_n$
1	1	1	0	1	0
1	1	0	1	Q_n	$\bar{Q}_n$
1	0	1	0	Q_n	$\bar{Q}_n$
1	0	0	1	0	1

If the truth table required is merely that shown earlier in Table 3, then the S_B and $\bar{S}_B$ inputs should both be held at 1, that is, these should be connected to the −4V rail, or otherwise held at −0·7V.

The inputs S_B and $\bar{S}_B$ may also be connected together and used as a second clock input. In this arrangement, setting of the bistable element by the signal can occur only when both clock pulses are present. In the absence of either clock pulse the output Q_{n+1} remains at Q_n.

The above description indicates the functions of the complete FKJ101 clocked set-reset staticisor. All of these functions could in practice also be derived from the FKJ111 J.K. flip-flop by making certain arrangements for providing suitable inputs. Under these conditions, however, the FKJ111 would give a considerably longer delay than the FKJ101 in performing the same function, and the S_A and $\bar{S}_A$ signals are both required. The FKJ111 also dissipates more power than the FKJ101. It is therefore not recommended that the FKJ111 should be used for ordinary set-reset clocked staticising.

Output of FKJ101

The duplicated outputs may be used in pairs separately, or combined. One pair already has 75Ω resistors internally connected. The other pair has no resistors connected, but two 75Ω resistors are available at other terminals and may be used with this second pair of outputs. If long lines are to be driven by the staticisor output then the outputs should be combined: the output then acts as a line driver (FKH121) with one resistor per output already connected. If only one pair of outputs is required, the unused outputs may be grounded leaving a single output resembling either FKH101 or FKH111.

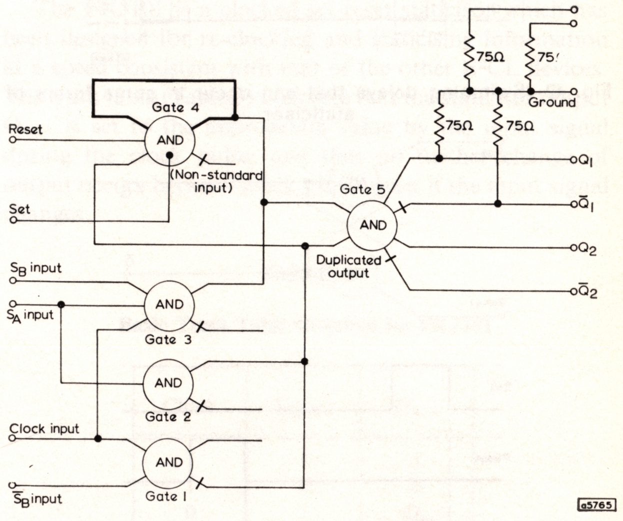

Fig. 45—Full logic diagram of FKJ101 for negative logic

DETAILS OF FKJ111

The FKJ111 is a J.K. flip-flop of the 'Master-Slave' type and is compatible in every respect with the other devices in the Mullard E²CL range, except that the encapsulation is different. Counting rates in excess of 100MHz are possible with the FKJ111.

Two particular problems which can arise in counting operations have been fully taken into account in the design of the circuit. These possible problems are,

(i) 'skew' in clock pulses, and

(ii) slow rise and fall times in the clock pulses.

The possibility of 'skew' between clock pulses at different points in the circuit may arise either because of the existence of different wired path-lengths for the clock pulse, or because of spreads in stage delay values. The error that can occur as a result of skew is shown in Fig. 46. Two conventional J.K. flip-flops (not FKJ111) are shown connected in cascade, and some skew is assumed to exist between the clock pulses applied to them. The waveforms show in negative logic the operation of such an arrangement, and show the error produced by the skew. With the J and K inputs to the first flip-flop held at 1, the output Q_1 should change once immediately following each clock pulse; the output Q_2 of the second flip-flop should change once immediately following each alternate clock pulse. The first flip-flop operates normally as is indicated by the waveform for Q_1, but errors occur in the operation of the second flip-flop. It can be seen that the output Q_1 changes value during the skewed clock pulse to the second flip-flop: therefore the second gate is capable of processing the new information when it should be processing the previous information. The errors that can occur during a change of $(J_2.\bar{Q}_2+K_2.Q_2)$ from 0 to 1, and the errors that can occur during a change from 1 to 0 are considered separately.

When Q_1 changes from 1 to 0, no problem arises provided that the 1 is present for sufficient time after the arrival of the skewed clock pulse, to allow the second flip-flop to latch on to this 1. If, however, the skew is so severe that the above condition is not satisfied, the second flip-flop will erroneously process the new information rather than the previous information. This difficulty will not occur unless the skew between the clock pulses is almost equal to the clock pulse duration, or is longer, whatever the duration of the clock pulse is.

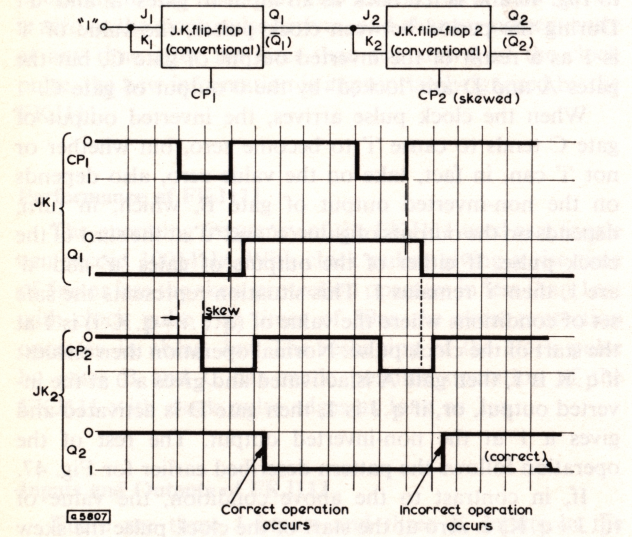

Fig. 46—Switching error that can occur with some forms of J.K. flip-flop

The situation when Q_1 is changing from 0 to 1 in the conventional J.K. flip-flop, imposes severe restrictions on the permissible clock pulse skew. The permitted clock pulse skew is very much less than the latch time of the flip-flop. The FKJ111 has been designed to overcome this problem by incorporating additional gating to ensure that the flip-flop is insensitive under those conditions which could otherwise cause this form of erroneous operation. This extra gating is described later. The gating detects the condition that $(J_2.\bar{Q}_2+K_2.Q_2)$ is equal to zero before the arrival of the clock pulse and locks the input gates so that any subsequent change of signal within the clock pulse period is ignored.

In the FKJ111, therefore, the permissible skew is limited by the previously discussed condition where Q_1 changes from 1 to 0 during the clock pulse. Thus, clock pulse skew with the FKJ111 can be permitted to be almost as great as the clock pulse duration.

Problems which can arise with clock pulses that have slow rise or fall times are also avoided in the FKJ111. This is achieved by reshaping the clock pulse by an E²CL gate before it is used internally in the flip-flop.

Simplified Logic Diagram of FKJ111

It was stated above that the FKJ111 is a 'Master-Slave' flip-flop: the master section acts on the leading (negative going) edge of the clock pulse, and the slave section acts on the trailing (positive going) edge of the clock pulse.

A simplified logic diagram is shown in Fig. 47, and this is used here to explain the ordinary action of the FKJ111. To enable a brief explanation of the flip-flop action to be given, a specific example is taken, that is, that J = 1 and K = 1 continuously. In addition it is

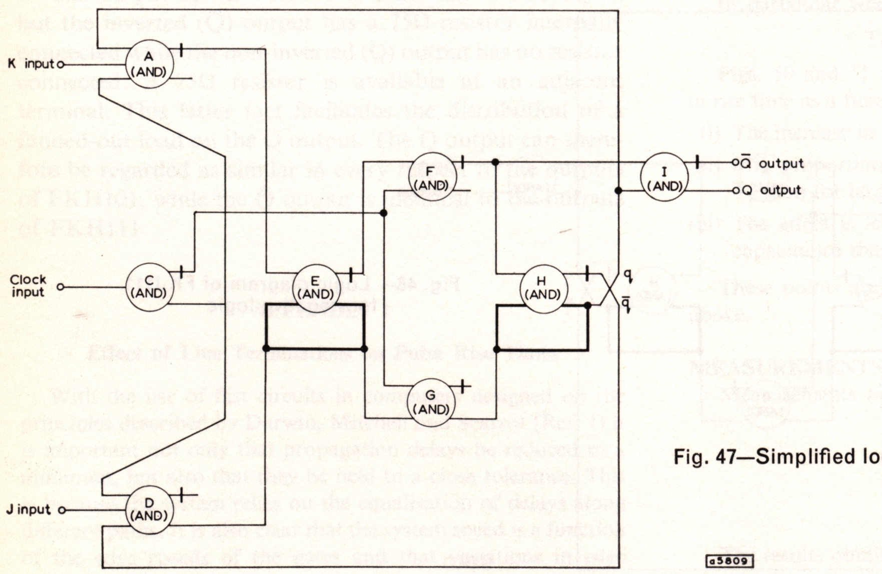

Fig. 47—Simplified logic diagram of FKJ111 for negative logic

assumed that the bistable elements E and H are set at zero at the beginning of the operation, that is, $q = Q = 0$ and $\bar{q} = \bar{Q} = 1$ at the beginning of the operation.

In the absence of a clock pulse, the gates A and D are both 'locked', that is, the non-inverted output of C is 0 and causes a 1 to appear at the inverted output of gates A and D (independently of the values of J, K, q and $\bar{q}$). Under these conditions the previous setting of gate E is left unchanged (as explained under FKJ101). The inverted output of gate E is therefore still its assumed value of 1 and the non-inverted output is 0.

During the next clock pulse the three inputs to gate D will be at 1. The non-inverted output of gate D is therefore 1. During this clock pulse the inverted output of gate A is also 1, because of the q input equal to zero. The state of the bistable element, gate E, therefore changes and gives an output of 1 at the non-inverted output and 0 at the inverted output. This change, however, cannot proceed via gates F and G during the clock pulse because both gate F and gate G are 'locked' by the 0 output from gate C in this period.

When the clock pulse is removed the output of gate G will change because it now has both inputs at 1. Gate F continues to have an inverted output at 1 because of the 0 input from E. Consequently, the bistable element, gate H, changes giving the new values $q = 1$ and $\bar{q} = 0$. At the same time the output gate I changes giving the new values $Q = 1$ and $\bar{Q} = 0$.

During the second clock pulse the condition of gate A will change, provided K is still assumed to be 1. This will reset E to zero. The output of gate I will again change on the removal of the second clock pulse after a similar train of events through the intermediate gates.

The output of gate I is seen, therefore, in this example to change from 0 to 1 or vice versa on the trailing edge of each clock pulse, while $J = K = 1$.

Gates A and D are 'locked' in the absence of the clock pulse, and gates F and G are 'locked' in the presence of the clock pulse. Therefore, whatever information is processed by the first part of the circuit during the clock pulse (leading edge) is processed by the second part of the circuit and the output gate only after the clock pulse is removed (trailing edge).

Protection Against Clock Skew

Protection against the effect of skew in the clock pulse is achieved in the FKJ111 by adding an extra gate and a small number of extra components to the simplified circuit shown earlier in Fig. 47. A simplified version of the logic diagram of the FKJ111 including the extra items is given in Fig. 48. It will be recalled that the most dangerous situation, which can lead to erroneous operation, occurs when $(J.\bar{Q}+K.Q)$ changes from 0 to 1 during the clock pulse: the way in which the possible resetting of gate E etc. is avoided under these conditions is explained in the following paragraphs.

The outputs from gate 'a' and 'd' are OR-ed. This OR-ed output is AND-ed with the clock pulse by gate B and then further OR-ed with the inverted clock output of gate C. The OR-ed output of gates B and C is called 'i' in Fig. 48 and is fed back as an input to gates 'a' and 'd'. During the period between clock pulses, the value of 'i' is 1 as a result of the inverted output of gate C, but the gates A and D are 'locked' by the 0 output of gate C.

When the clock pulse arrives, the inverted output of gate C tends to cause 'i' to become zero, but whether or not 'i' can, in fact, take on the value zero, also depends on the non-inverted output of gate B, which, in turn, depends on the outputs of gates 'a' and 'd' at the start of the clock pulse. If either of the outputs of gates 'a' and 'd' are 1, then 'i' remains 1. This situation represents the safe set of conditions where the value of $(\bar{q}.J.i+q.K.i)$ is 1 at the start of the clock pulse. Normal operation then ensues: if $q.K$ is 1, then gate A is activated and gives a 0 at the inverted output, or, if $q.J$ is 1, then gate D is activated and gives a 1 at the non-inverted output. The rest of the operation follows the pattern described earlier for Fig. 47.

If, in contrast to the above condition, the value of $(\bar{q}.J+q.K)$ is zero at the start of the clock pulse the skew protection circuit operates to stop the flip-flop responding to a later change within the clock pulse period. When $(\bar{q}.J+q.K)$ is zero, then the outputs of both gate 'a' and gate 'd' are at zero. If, while this condition exists, the clock pulse arrives then the OR-ed outputs of gates B and C can take on the value zero, that is, $i = 0$. Since 'i' is fed into gates 'a', 'd', the gates A and D are locked. The output from gate A and the output from gate D are unchanged and this ensures that the state of gate E, and hence the outputs Q and $\bar{Q}$ of the FKJ111 are therefore unchanged. This locked condition persists until the clock pulse is removed and 'i' returns to the value 1. Consequently, any change of $(\bar{q}.J+q.K)$ from 0 to 1 within the clock pulse period produces no response and is ignored, and so the flip-flop is immune to the problem arising from skew in the clock pulse.

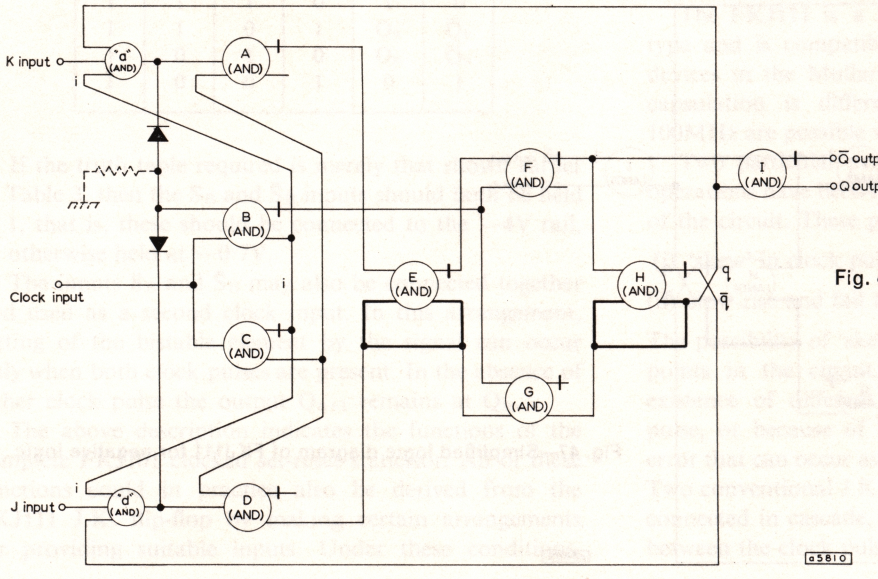

Fig. 48— Logic diagram of FKJ111 for negative logic

It was stated above that Fig. 48 is a simplified diagram. In fact, the gates 'a' and 'd' are not separate gates: the logic function indicated in Fig. 48 is obtained by fan-outs from the input emitter followers of gates A and D.

The skew protection and lock-out system is very fast, operating in less than 1ns. This means that if $(q.J+\bar{q}.K)$ is zero as the clock pulse arrives, and changes subsequently at any time after 1ns later than the arrival of the clock pulse, the new information is appropriately ignored by the FKJ111.

Performance of FKJ111

The operating frequency of the FKJ111 used as a toggle can exceed 100MHz. With clock pulses giving a rise time of 5ns or less the skew protection operates in less than 1ns: with clock pulse rise times of 50ns the skew protection operates in about 3ns. The reshaping of the clock pulse by gates B and C has made possible operation of the FKJ111 with clock pulse edges as long as 2μs.

Inputs and Outputs of FKJ111

There are three J inputs and three K inputs in the FKJ111; each set of inputs are AND-ed by the input gates. There are also inputs for Clock, Set and Reset.

The output of the FKJ111 is a normal E²CL output, but the inverted ($\bar{Q}$) output has a 75Ω resistor internally connected while the non-inverted (Q) output has no resistor connected: a 75Ω resistor is available at an adjacent terminal. This latter fact facilitates the distribution of a fanned-out load on the Q output. The Q output can therefore be regarded as similar in every respect to the outputs of FKH101, while the $\bar{Q}$ output is identical to the outputs of FKH111.

APPENDIX 1

Effect of Line Terminations on Pulse Rise Times

With the use of fast circuits in computers designed on the principles described by Darwin, Mitchell and Scarrot (Ref. 1) it is important not only that propagation delays be reduced to a minimum, but also that they be held to a close tolerance. This is because the system relies on the equalisation of delays along different paths. It is also clear that the system speed is a function of the edge speeds of the gates and that variations in edge speeds are equivalent to an increased spread on propagation delay. It is the purpose of this Appendix to show that the edge speed depends on the method of inter-connection used as well as on the inherent characteristics of the gates.

THEORY

Consider a step waveform travelling along a line and meeting a capacitive termination C (Fig. 49a). The voltage across C will change with time constant CZ_o and will thus have a rise time $2{\cdot}2\times CZ_o$. If the incident pulse is not a step but has a finite rise time T_p then the total rise time (T_{to}) of the output is given approximately by the equation

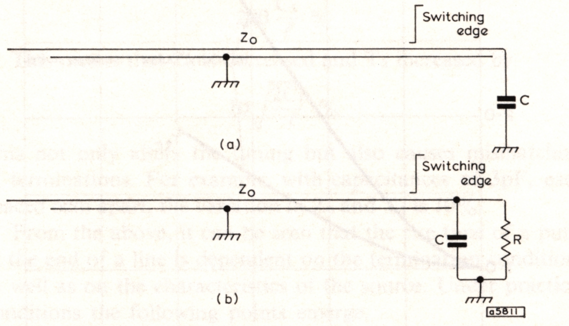

Fig. 49—Step waveform travelling along a transmission line terminated by:

(a) a capacitance, and

(b) a capacitance shunted by a resistance

$$T_{to} = \sqrt{T_p^2+(2{\cdot}2\times CZ_o)^2}$$

Next consider the case when the capacitance is shunted by a resistor R (Fig. 49b). It may be readily shown that the time constant is now

$$C\left[\frac{Z_oR}{Z_o+R}\right],$$

and thus the rise time for a step input is

$$2{\cdot}2\times C\left[\frac{Z_oR}{Z_o+R}\right].$$

The rise time (T_{tR}) for a finite incident pulse is, by analogy with the previous case,

$$T_{tR} = \sqrt{T_p^2+\left[2{\cdot}2\times C\left(\frac{Z_oR}{Z_o+R}\right)\right]^2}$$

In particular when $R = Z_o$ this becomes

$$T_{tr} = \sqrt{T_p^2+[1{\cdot}1\times CZ_o]^2}$$

Figs. 50 and 51 show the actual and proportional increase in rise time as a function of C. It is clear that

(i) The increase in rise time becomes greater as C increases

(ii) The proportional increase is greater for small values of T_p than for large.

(iii) The effect is less when the resistor is present across the capacitance than when it is absent.

These points are also directly deducible from the equations above.

MEASUREMENTS

Measurements were made with the following conditions:

$Z_o = 50\Omega$
$T_p = 1\text{ns}$
$R = 56\Omega$
$C = 33\text{pF}$

The results obtained, are shown in Table 4.

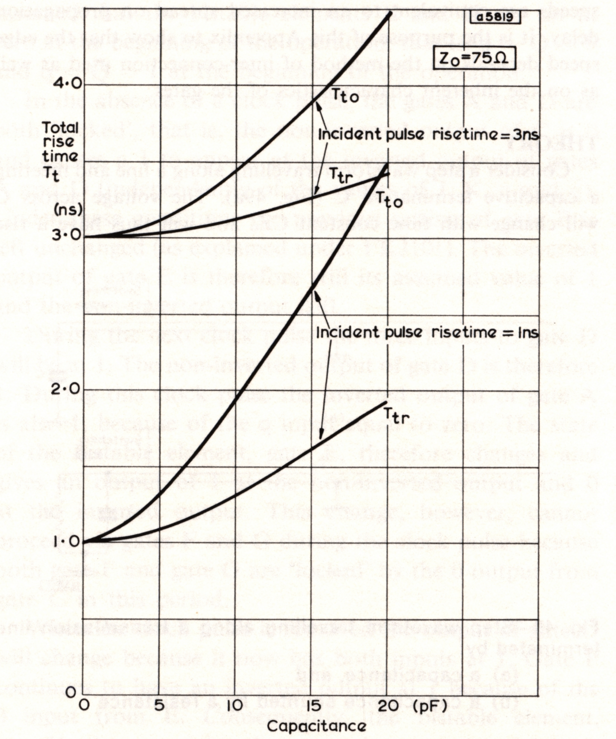

Fig. 50—Increase in rise-time as a function of capacitance

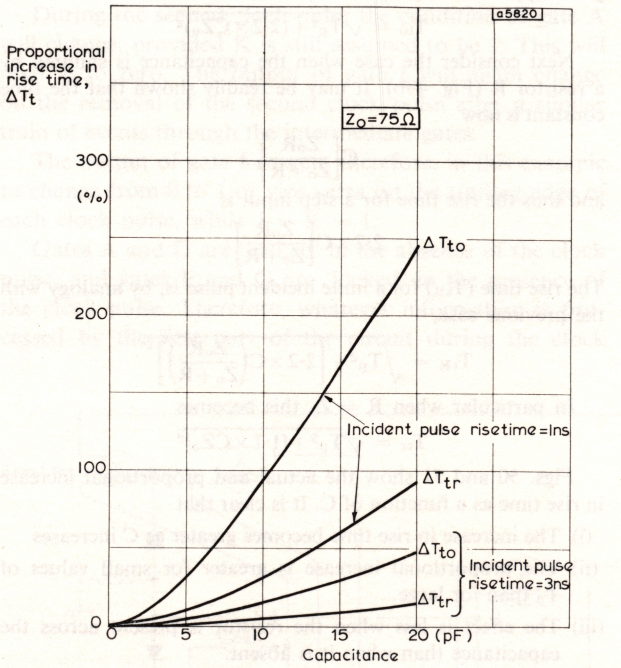

Fig. 51—Proportional increase in rise-time as a function of capacitance

TABLE 4
Measured and Calculated Rise Times

	Measured	Calculated
T_{to}	4·2ns	3·8ns
T_{tR}	2·4ns	2·16ns

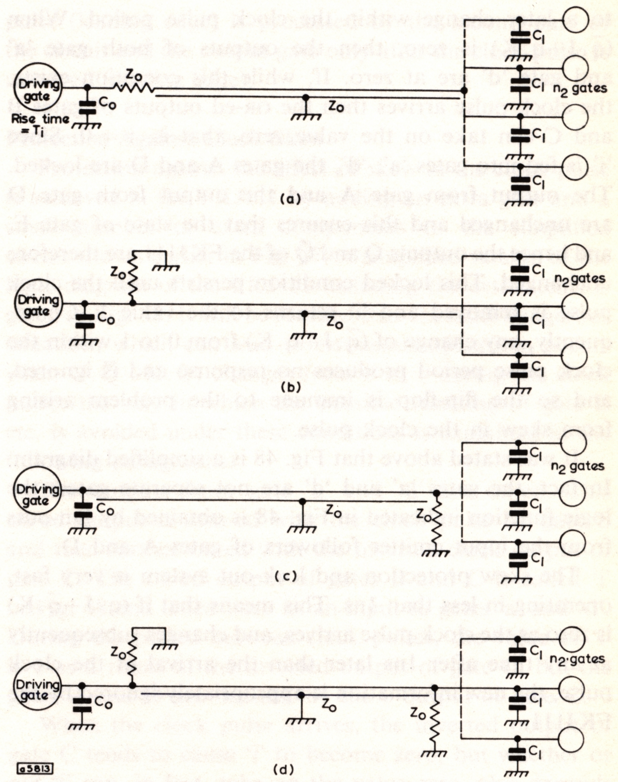

Fig. 52—Possible arrangements for driving transmission lines

The measured values were increased by pulse edge aberrations caused by the finite sizes of the terminating components.

APPLICATION TO PRACTICAL CASES

Fig. 52 shows the possible arrangements for driving lines. Additional gates may be tapped along the lines, as well as those at the far ends.

Of these methods, the serial-drive case can only be used for driving from a voltage source, and the others will normally be used only with a current source.

The circuit of Fig. 52a can thus be transformed into that of Fig. 53a. The capacitance of C_o does not affect the rise time of the pulse transmitted along the line since the voltage source provides sufficient current to charge C_o in the same time as the intrinsic rise time of the source. The transmitted pulse thus has rise time T_i. If no gates are tapped along the line the output rise time is given by the expression

$$\sqrt{T_i^2+[2{\cdot}2\times n_2C_iZ_o]^2}$$

If gates are tapped randomly, then at each tapping point the pulse sees an effective termination of C_i and Z_o (it is also assumed that no two gates are close enough together to appear as one load). Thus for n_1 such gates the total rise time of the output pulse is given by the expression

$$\sqrt{T_i^2+n_1[1{\cdot}1\times C_iZ_o]^2+[2{\cdot}2\times n_2C_iZ_o]^2}$$

The third term is larger than the second unless

$$n_1 \geqslant 4n_2^2.$$

Therefore, tapping along the line has less effect than grouping circuits at the far end.

Similarly Fig. 52b can be transformed into Fig. 53b. This is different from Fig. 53a because C_o is placed after Z_o instead of before it. If C_o were reduced to zero the two forms would become equivalent.

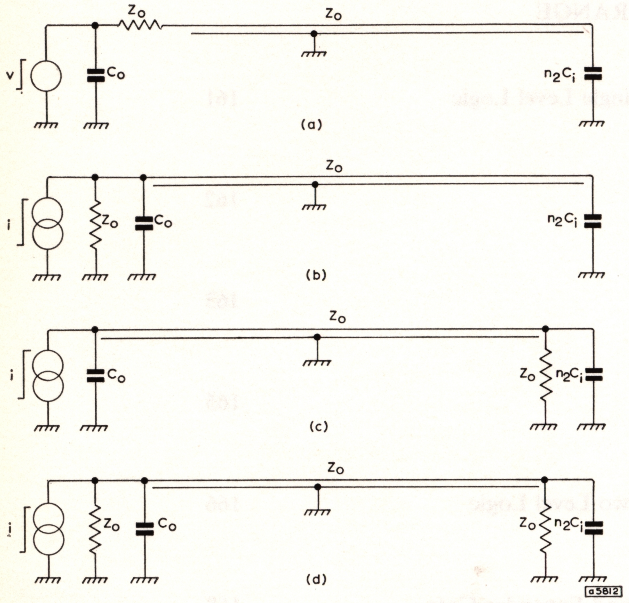

Fig. 53—Equivalent circuits of the arrangements which Fig. 52 shows

The rise time of the pulse transmitted along the line is now given by the expression

$$\sqrt{T_i^2+[1{\cdot}1\times C_oZ_o]^2}$$

The degradations along the line and at the end are the same as previously so that the output pulse has rise time equal to

$$\sqrt{T_i^2+[1{\cdot}1\times C_oZ_o]^2+n_1[1{\cdot}1\times C_iZ_o]^2+[2{\cdot}2\times n_2C_iZ_o]^2}$$

In practice, since Fig. 52b is the standard configuration for use with a current source, the edge speed would be that propagated into the line in this case. Thus for comparable circuits

$$T_{i(\text{voltage source})} = \sqrt{[T_{i(\text{current source})}]^2+[1{\cdot}1\times C_oZ_o]^2}$$

The two configurations then become completely equivalent.

Fig. 52c is equivalent to Fig. 53c: the termination is at the opposite end to that in Figs. 52b and 53b. By a similar argument to that in the previous case, the output rise time is given by

$$\sqrt{T_i^2+[2{\cdot}2\times C_oZ_o]^2+n_1[1{\cdot}1\times C_iZ_o]^2+[1{\cdot}1\times n_2C_iZ_o]^2}$$

This is less than for termination at the near end, unless

$$[2{\cdot}2\times C_oZ_o]^2+[1{\cdot}1\times n_2C_iZ_o]^2 \geqslant [1{\cdot}1\times C_oZ_o]^2+[2{\cdot}2\times n_2C_iZ_o]^2,$$

that is, unless

$$n_2 \leqslant \frac{C_o}{C_i}$$

Thus, if C_o is 8pF and C_i is 3pF, termination at the far end, when more than two gates are grouped at the end of the line, gives a faster edge than is given by the termination at the sending end.

Combining Figs. 53b and 53c gives Fig. 53d as the equivalent circuit of Fig. 52d. By analogous arguments to those previously given, the output rise time is given by

$$\sqrt{T_i^2+[1{\cdot}1\times C_oZ_o]^2+n_1[1{\cdot}1\times C_iZ_o]^2+[1{\cdot}1\times n_2C_iZ_o]^2}$$

Hence, the line driver configuration produces the fastest edge speed for a given set of conditions.

If the tapping points are close enough for the loading to be considered uniform, the result is to reduce the effective value of Z_o and increase the propagation delay rather than to degrade the edge speed.

The characteristic impedance (Z_o) is given by

$$Z_o = \sqrt{\frac{L}{C}}\ \Omega,$$

and the propagation delay (T_d) is given by

$$T_d = \sqrt{LC}\ \text{s/m}$$

For a 75Ω printed line the capacitance, C, is approximately 50pF/m.

Consider capacitances C_i each, at ℓcm apart but close enough to act as a uniform load. Then the new capacitance of the line is

$$50\left(1+\frac{2C_i}{\ell}\right)\ \text{pF/m}$$

Thus, the increase in C is

$$200\,\frac{C_i}{\ell}\ \%$$

This means that Z_o is decreased and T_d increased by

$$10\sqrt{\frac{2C_i}{\ell}}\ \%$$

This not only alters the timing but also causes mismatching of terminations. For example, with capacitances of 3pF, each spaced 6cm apart, the variation in Z_o and T_d is 10%.

From the above, it can be seen that the rise time of a pulse at the end of a line is dependent on the termination conditions as well as on the characteristics of the source. Under practical conditions the following points emerge.

(i) The input capacitance, C_i, of a gate should be as low as possible. As mentioned earlier, this is one of the major advantages of E²CL.

(ii) The major part of the pulse degradation is caused by the cluster of gates at the end of the line.

(iii) In practice, serial drive from a voltage source is equivalent to parallel drive from a current source when the termination is at the sending end.

(iv) The edge is faster for termination at the far end than it is for termination at the sending end, unless the number of gates at the far end is less than the ratio

$$\left[\frac{\text{Output capacitance of gate}}{\text{Input capacitance of gate}}\right]$$

(v) The line driver gives the fastest edge for a given set of conditions.

The effect of tapping along a line, in such a way that the load may be considered as uniform, has also shown that it is important that C_i be small, or mismatch and timing errors become significant.

REFERENCE 1

Darwin, G. P., Mitchell, R. W., Scarrot, G. G., 'Fast Arithmetic Systems Constructed from General Purpose Logical Elements'. **1966 British Joint Computer Conference. I.E.E. Publication No. 19**, pp. 204-211.

Mullard thank the I.E.E. for permission to reproduce part of the information given in a paper entitled 'Problems Encountered in the Integration of a 100MHz Counting Circuit' by G. T. Dove, G. T. Lloyd and A. R. Rao (Mullard Ltd.), presented at the I.E.E. Integrated Circuits Conference (Conference Publication No. 30), Eastbourne, May 1967.

This article describes a range of integrated logic elements which are being developed. Only some of the devices are currently available; the others will become available during 1967.

The circuits described are being developed in association with the Westinghouse Molecular Electronics Division, Maryland, U.S.A.

THE E²CL RANGE

FKH111 Dual AND-with-NAND Gate for Single Level Logic 161

FKH161 Twin Output Gate 162

FKH121 Single Line Driver 163

FKH141 Dual Line Receiving Unit 165

FKH101 Dual AND-with-NAND Gate for Two Level Logic 166

FKH131 Single 8-Input Two Level Logic and Expander Gate 168

FKH171 Single 8-Input Two Level Logic Unit giving OR-ed AND 169

FKL101 Interface Unit 170

FKJ101 S.R. Clocked Staticisor 172

FKJ111 J.K. flip-flop 174

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Additional Information

COIL DETAILS FOR COLOUR-DIFFERENCE DECODER

All coils except L_4 are wound on Brayhead formers type P1011/1, with Neosid $4\times0{\cdot}5\times12{\cdot}7/900$ screw cores. Coil L_4 is wound on $\frac{1}{4}$in S.R.B.P. tube with a Ferroxcube core type FX1068 mounted in an adjustable sleeve.

The wire used for L_1, L_2, L_3 and L_4 is 42 s.w.g. en. Cu., the numbers of turns being 70 (L_1), 55 (L_2), 30 (L_3) and 1700 (L_4).

The wire used for L_5, L_6, L_7, L_8 and L_{10} is 42 s.w.g. en. Cu. silk-covered, the numbers of turns being 120 (L_5), 120 (L_6), 250 (L_7), 80 (L_8) and 90 (L_{10}).

Windings L_4, L_5, L_6, L_7, L_8 and L_{10} are $\frac{1}{4}$in wide, and the winding gears are 50–32–44–36–40–80.